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Elektor Electronics

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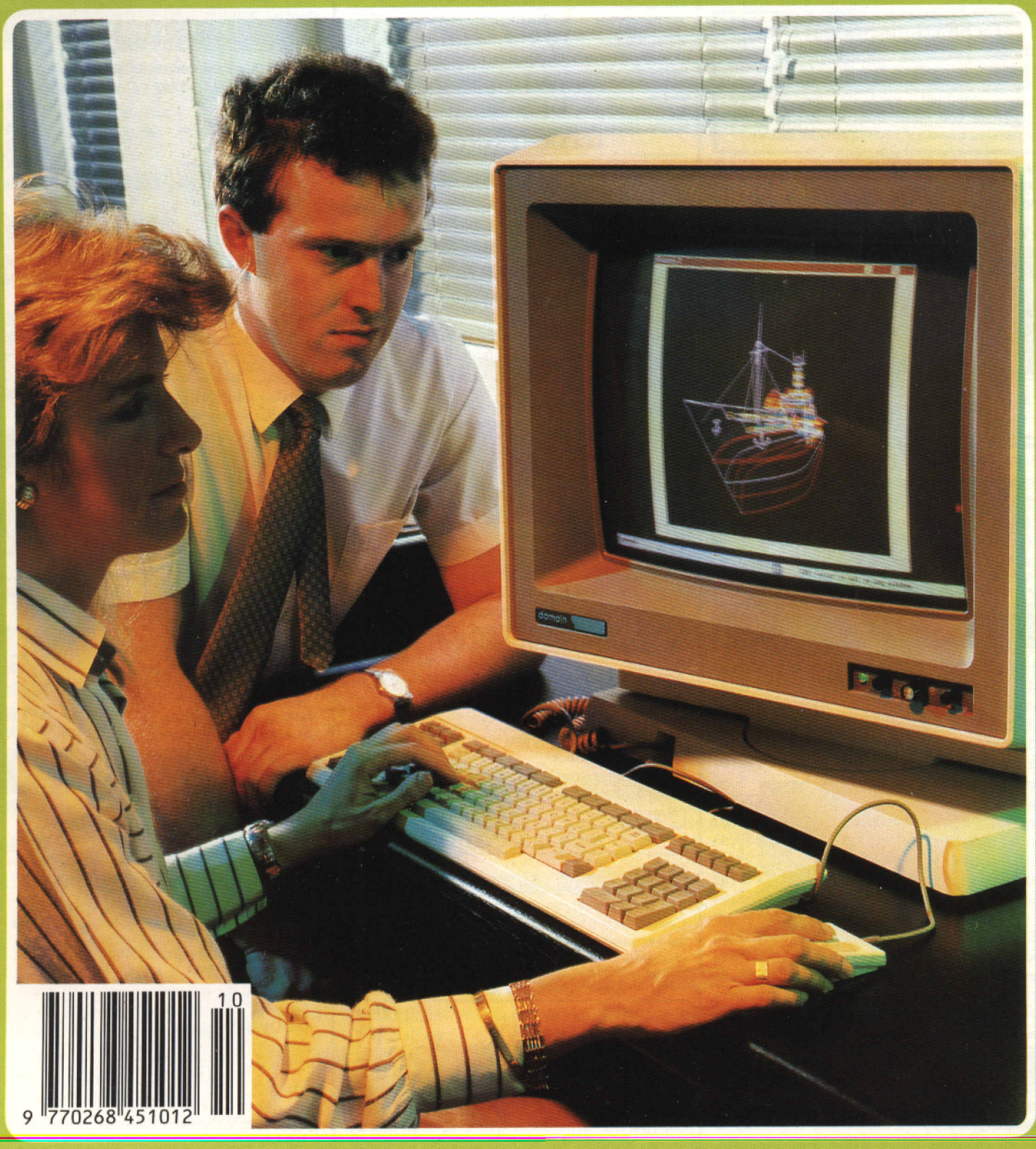
Open systems
Log-antilog amplifier
Logic analyser for Atari ST
16-channel running lights



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Elektor Electronics

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October 1989
Volume 15
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Theme of the month in November will be Microprocessors and Computers

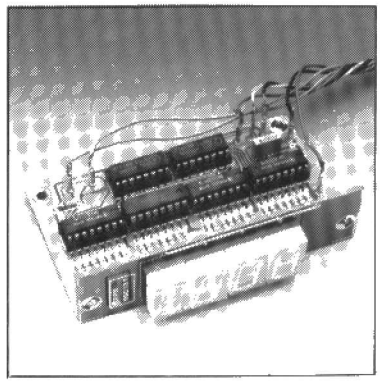
Also in the November issue:

- Extension card for Archimedes
- CMOS preamplifier
- 8098 evaluation board
- 3 1/2 LED-digit SMD voltmeter
- EPROM simulator
- Speeding up the computer
- Multiplex control with U6050/6052
- Computer mouse

We regret that owing to circumstances beyond our control neither "SAVE decoder" nor "Dark-room clock" could be published this month.

Front cover

Automation in the British industry is booming. The vast majority of factories in the UK now have some form of automation or computer-aided design facilities. Engineers are shown here using a 3D modelling system at the Strathclyde Institute in Glasgow, which has recently set up a new centre for computer integrated manufacture (CIM). It is Britain's first wholly independent CIM establishment and is claimed to be the largest of its kind in Europe.



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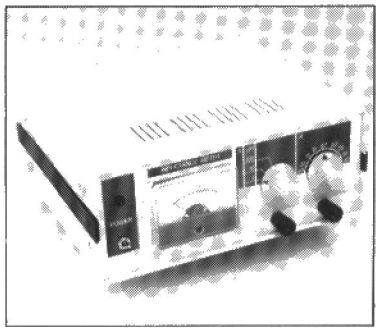

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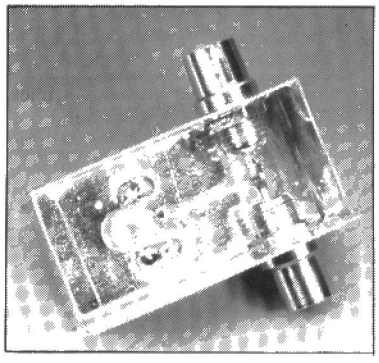

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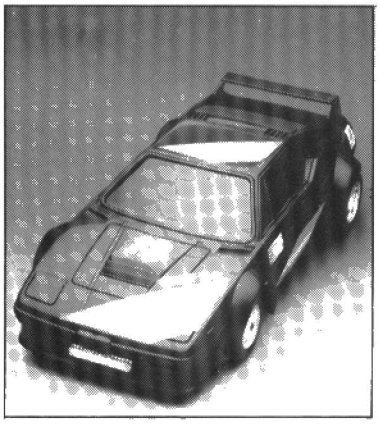

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CABLE TV: A RENAISSANCE?

The British cable television industry died a premature death in the early 1980s, whereas that in the USA and continental Europe continued to thrive. The reasons for the failure in Britain were twofold. Firstly, the operating costs of the 'wired society' proved much higher than budgeted. Secondly, and perhaps more importantly, the cable companies could not provide enough new channels to tempt viewers to hire a cable terminal. In contrast, many viewers in North America had a choice of more than 50 channels and those in western Europe of up to 20 or so.

British viewers, after the Americans the most ardent television watchers in the world, want more television. They want more choice like viewers in North America and continental Europe. What they want in particular is more feature films – and they are prepared to pay for it. This is borne out by the staggering fact that the British spend close to £1 billion a year on buying and renting video cassettes (in Britain, there are more VCRs per household than anywhere else in the world).

To meet these demands, British satellite TV was born. Early this year, Sky Television started to beam down the first of its planned programmes via the Luxembourgian satellite *Astra*, while British Satellite Broadcasting is planning to launch its programmes early next year. Together, these two operators will eventually provide (according to current planning) up to ten additional television channels. Not surprisingly, there is intense rivalry between the two.

Unfortunately for the viewer, Sky has chosen to cling to the outdated PAL system (undoubtedly to be first on the air), whereas BSB has opted wisely, at least from a long-term point of view, for the superior MAC system. Viewers will, therefore, be able to receive the programmes from only one of the two satellites direct, unless they install two different receivers and aerials.

No doubt, most viewers will decide, wherever possible, to be connected to a cable system (at an average cost of just under £20 per month) that shows the programmes of both Sky and BSB in preference to cluttering up their homes with two sets of different equipment (at a cost of at least £300 per set). Ironically, therefore, the cable television industry is being reborn from the rivalry between the two satellite operators.

The satellite operators should, however, find some consolation in the fact that cable television will allow, or at least help, them to make a profit in the lifetime of their shareholders, who have already invested close to £1 billion and are being asked for more. Some observers think it highly unlikely that, without the income from cable television, the two satellite operators will be able to break even in the next 20 years. They estimate that the break-even point (assuming both operators survive) will be reached at a market penetration of about 30%, which is equivalent to more than six of the 21 million homes in Britain being able to receive the two sets of programmes. They believe that this level of penetration will not be reached, if at all, until well into the next century and some feel, therefore, that neither of the two organizations will break even until one has been forced out of the race.

Who that will be is anybody's guess. Both competitors have a fair chance of survival, since both have some unique advantages: Sky commercial ones and BSB political and technical ones. BSB's satellite will probably deliver a slightly better picture and its smaller dish will be easier to install and be less obtrusive. Both operators should bear in mind, however, that viewers want to be able to choose between programmes, not technologies, so that, if North America is anything to go by, the company with the best movie channel will win. Based on the current situation, our view is that the real winner, at least in the short to medium term, will be Britain's cable television industry. And let us not forget that if and when one of the satellite operators is forced out, there will be another loser: the British viewing public.

CD ERROR DETECTOR

T. Giffard

As almost any owner of a CD player must have noted at some time, serious scratches and other surface irregularities on compact discs cause sound reproduction errors that are beyond the capabilities of the error correction circuits in the player. The present circuit gives a reliable indication of the quality of the CD by counting the number of playback errors.

The degree of redundancy built into the digital coding system used for compact discs allows complex electronic circuitry to detect and correct many errors as the disc is playing. The actual correction operations go unnoticed by the listener, but do have their practical limits.

The present error detector is a 4-digit counter with a maximum count of 9999. The circuit is suitable for use with any CD player that incorporates signal processing ICs of the second or third generation from Philips Components.

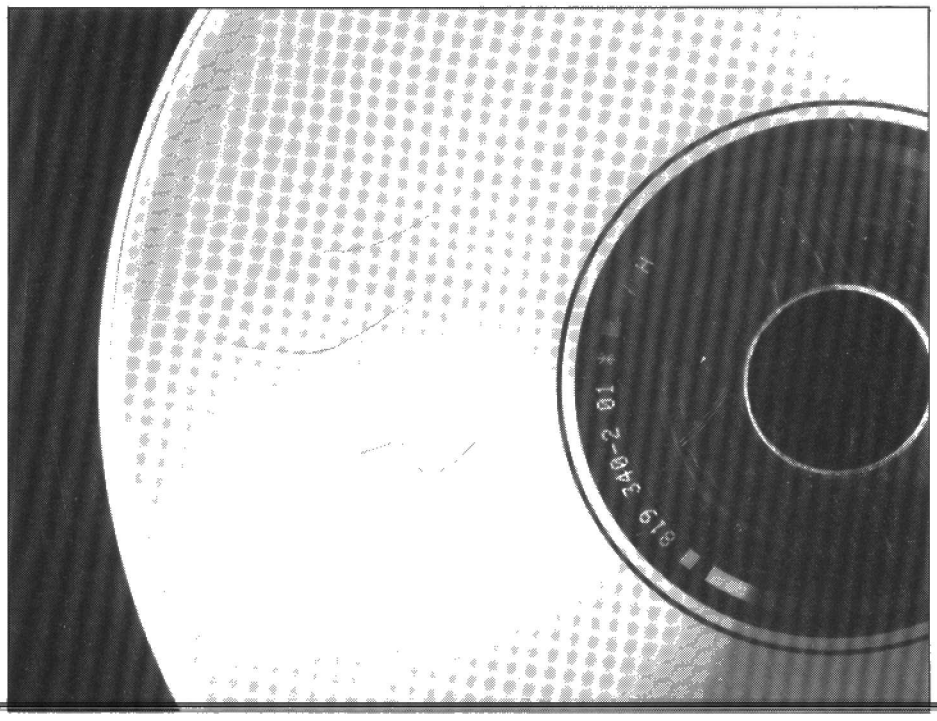
The counter is connected to the error detection output on the laser control and error correction system of the CD player, and indicates the number of times the laser detects a scratch, a hole in the metallized surface, or any other surface irregularity on the disc. Evidently, the higher the read-out of the error detector, the lower the quality of the compact disc.

Error correction in a CD player

The laser that scans the disc surface supplies a high-frequency signal from which the digital information is recovered. The block diagram of a second-generation CD player from Philips (Fig. 1) shows that the amplification of this signal is one of the functions of the TDA5708, which also serves to control and focus the laser. The TDA5708 signals the presence of large errors in the HF signal to the decoding IC, which responds by starting an error correction process. The TDA5708 also ensures that the information formed by the microscopic holes in the CD surface is correctly read. This function is required to compensate the laser scanning operation if the size of the holes is found to be outside certain limits.

Errors may also arise from incorrect control of the play mechanism. These errors are, of course, not caused by the disc, but by the CD player, whose alignment may need re-adjusting. Unfortunately, these errors are not found in the error detection signal supplied by the TDA5708.

The HF output signal of the TDA5708 requires quite some processing before an audio signal is available. As shown in Fig. 1, four ICs are used to accomplish this: an SAA7210, an SAA7220, a TDA1541 and a TDA1542. Of these, the SAA7210 performs the bulk of the error correction. The SAA7220 contains the oversampling filter and an interpolation circuit for errors that can not be corrected by the SAA7210. Only the SAA7210 and SAA7220 are relevant to the operation of the present error detector.



The SAA7210 performs error correction on the basis of the Cross-Interleaved Reed-Solomon Code (CIRC), adopted as part of the Philips/Sony standard for compact disc players. In principle, the system can handle the correction of a maximum of 4,000 successive bits, although this number is increased to 12,300 by means of interpolation. In practice, this means that virtually all small errors, such as digital pattern irregularities caused by disc production errors, can be corrected by this IC. The SAA7210 uses a RAM buffer for data storage and correction. If correction is impossible, a simple interpolation operation is performed. Should this also exceed the error correcting capabilities, the SAA7210 prompts the SAA7220 to interpolate a maximum of 8 successive datawords. The audio output of the CD player is only muted when all correction mechanisms fail because of a totally unrecoverable error.

It would be interesting to count the actual number of times the error correction circuit is actuated, but this is, unfortunately, not so simple in view of the high degree of integration of the currently used IC sets in CD players.

Looking at the error detection systems that produce accessible signals, the HFD (high-frequency Detector) output of the TDA5708 appears to be suitable. It should be noted that although some Philips CD players do not have a TDA7508, the HFD signal is usually fairly simple to find with the aid of a circuit diagram. The HFD output is actuated when the signal supplied by the laser diode drops considerably as a result of a serious error on the disc. This makes the HFD output signal suitable for driving the error detector circuit. As already stated, the HFD signal is used to signal to the SAA7220 that an error has been detected that needs correcting.

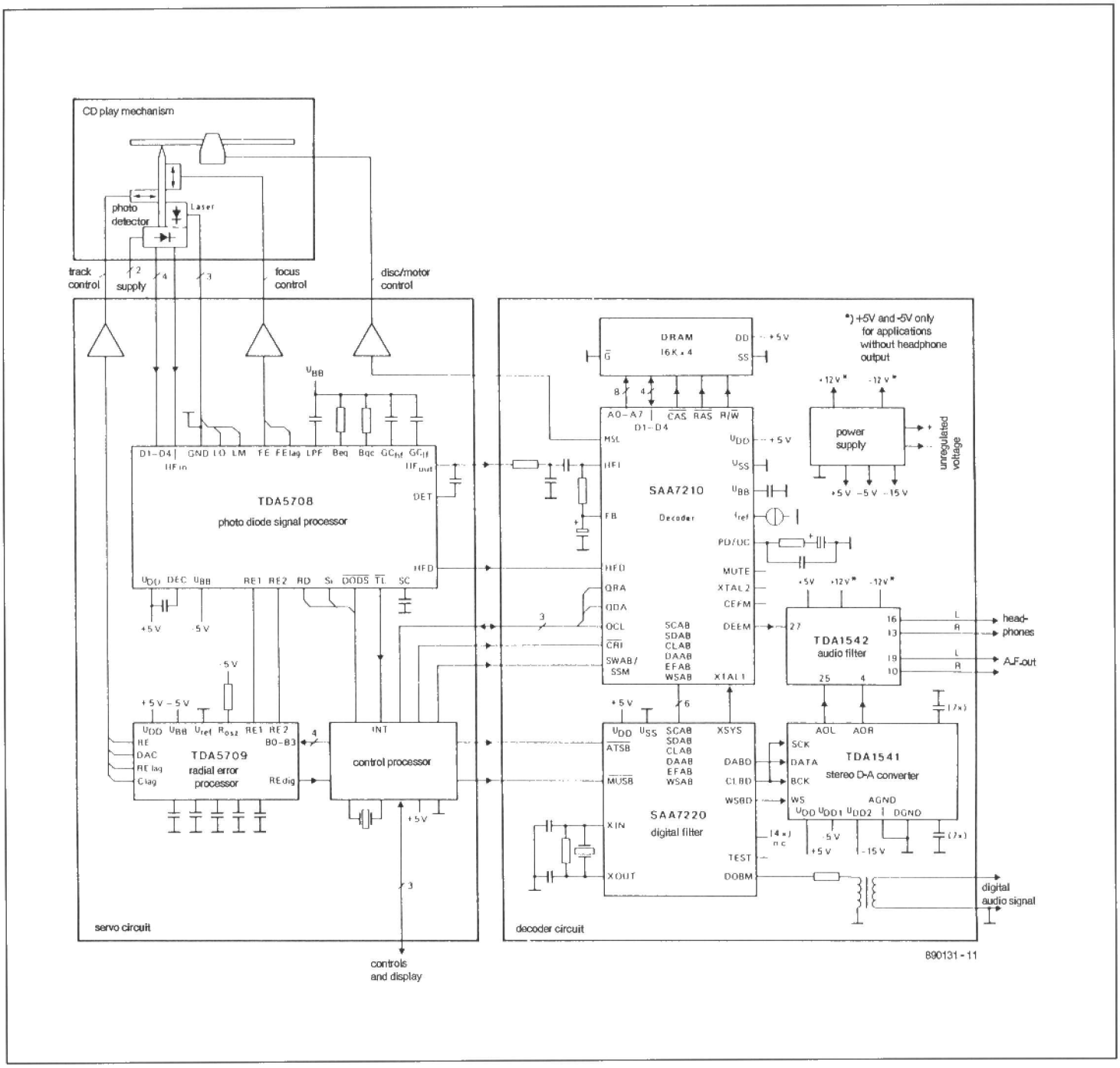


Fig. 1. Block diagram of a typical compact disc player based on Philips Components' second and third generation of CD decoder chips.

The counter: simple as can be

The circuit diagram of the CD error detector is given in Fig. 2. Only six ICs are used. Four common-anode LED displays are driven by open-collector display drivers Type 74LS247. This IC is used here because it provides ripple blanking and neat indications of the numbers 6 and 9, avoiding 'b' and 'q' like appearances respectively. A disadvantage of the 74LS247 is the lack of an internal latching register, which complicates multiplexing considerably. Multiplexing is, therefore, not used in the circuit, obviating the possible risk of interference by fast changing digital signals.

The maximum current consumption of the LED read-out is reached when four digits '8' are displayed. This combination requires a supply current of 4×7×10 mA = 280 mA. The use of high-efficiency displays allows the segment current to be reduced drastically by changing resistors R_1 through R_{28} to, say, 1 kΩ types.

The Q outputs of counters IC_5 and IC_6 are connected direct to the inputs of the display drivers. The read-out circuit is set up to provide leading zero suppression: an error count of, for example, 8 is displayed as '8', not '0008'.

The counter circuit has 3 input terminals. The connection of the ground terminal is straightforward because it goes to a grounded point in the CD player, near the SAA7210 or SAA7220. Input terminal A of the counter circuit is connected to the MUTE signal that should be available in any modern CD player. The MUTE signal is active when the laser assembly is moved, so that audible noise then generated is effectively suppressed. In the counter circuit, the MUTE signal is used to disable the counters and prevent false readings as the laser is repositioned. Input B, finally, is connected to the HFD pin of the SAA7220. Provided the MUTE signal is not active, the counter is incremented at each pulse on the HFD line.

The 4 counters used in the circuit are housed in two ICs Type 4518. The counters are linked via their Q3 outputs to form a cascade capable of counting up to 9999 clock (HFD) pulses. Such a high error count should, however, be rare.

Switch S_1 allows the counter to be cleared, which is useful if several discs are played in succession. The switch takes the RST inputs of all 4 counters high. An automatic reset of the circuit at power-on may be achieved by fitting a 100 nF capacitor across S_1.

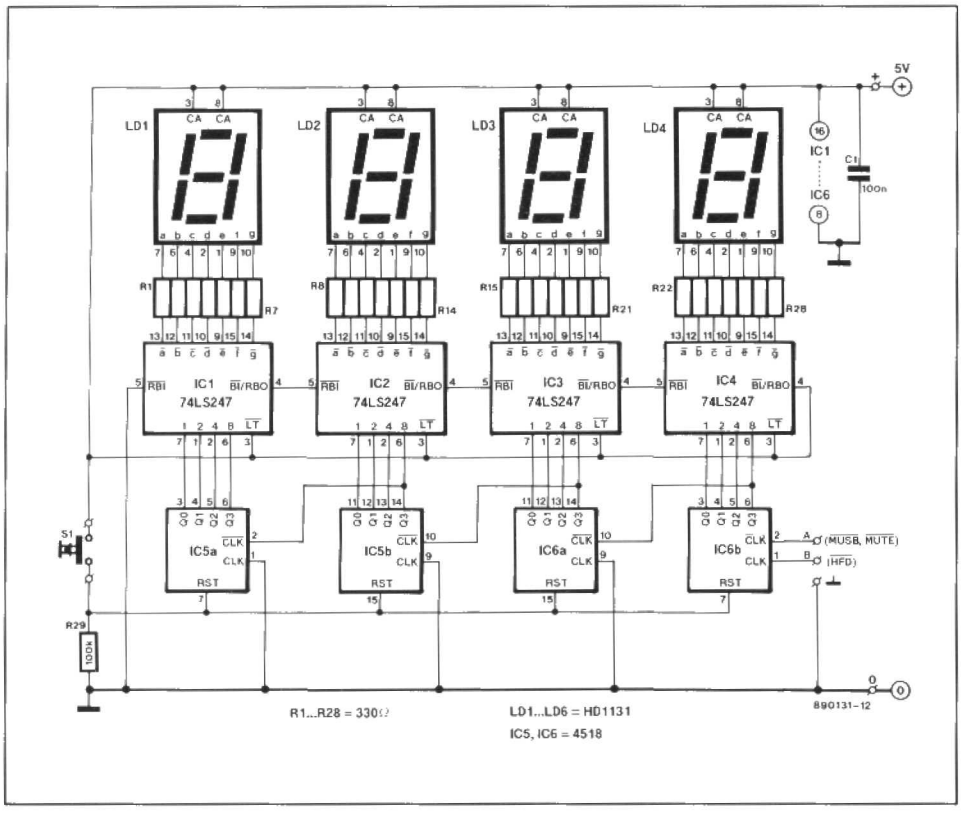


Fig. 2. Circuit diagram of the 4-digit error detector for compact disc players.

Construction

The lay-out of the compact printed-circuit board for the error detector is shown in Fig. 3. Cut off the display section of the board so that it can be mounted vertically on to the main board by means of short pieces of solid wire, as illustrated by the photograph of Fig. 4. Do not cut off the display section if you want to install the detector in the top panel of the CD player.

All parts are mounted on to the PCB. Do not damage the LED displays by soldering them direct on to the PCB — instead, use a single 40-pin IC socket to hold them all.

Make the right connections

The circuit was designed and tested by connecting it to a Philips CD player with the previously mentioned chip set. First-generation versions or players from other manufacturers may have other chips or even discrete circuits. The service documentation with such a CD player should enable the two necessary control signals, HFD and MUTE, to be found.

Connecting the error detector to a CD player with a SAA7210 is simple. Figure 5 shows the pin-out of this IC. Ground is connected to pin 20, MUTE to pin 11 and HFD to pin 26. If there is also a SAA7220 in the player, the MUTE signal of the SAA7210 is usually not connected. If this is the case, use the MUSB signal at pin 23 of the SAA7220.

Parts list

Resistors:
$R_1 - R_{28} = 330\Omega$
$R_{29} = 100k$

Capacitor:
$C_1 = 100n$

Semiconductors:
$LD_1 - LD_4$ = HD1131 (common-anode; Siemens).
$IC_1 - IC_4$ = 74LS247
IC_5;IC_6 = 4518

Miscellaneous:
S_1 = push-to-make button.
PCB Type 890131 (see Readers Services page).

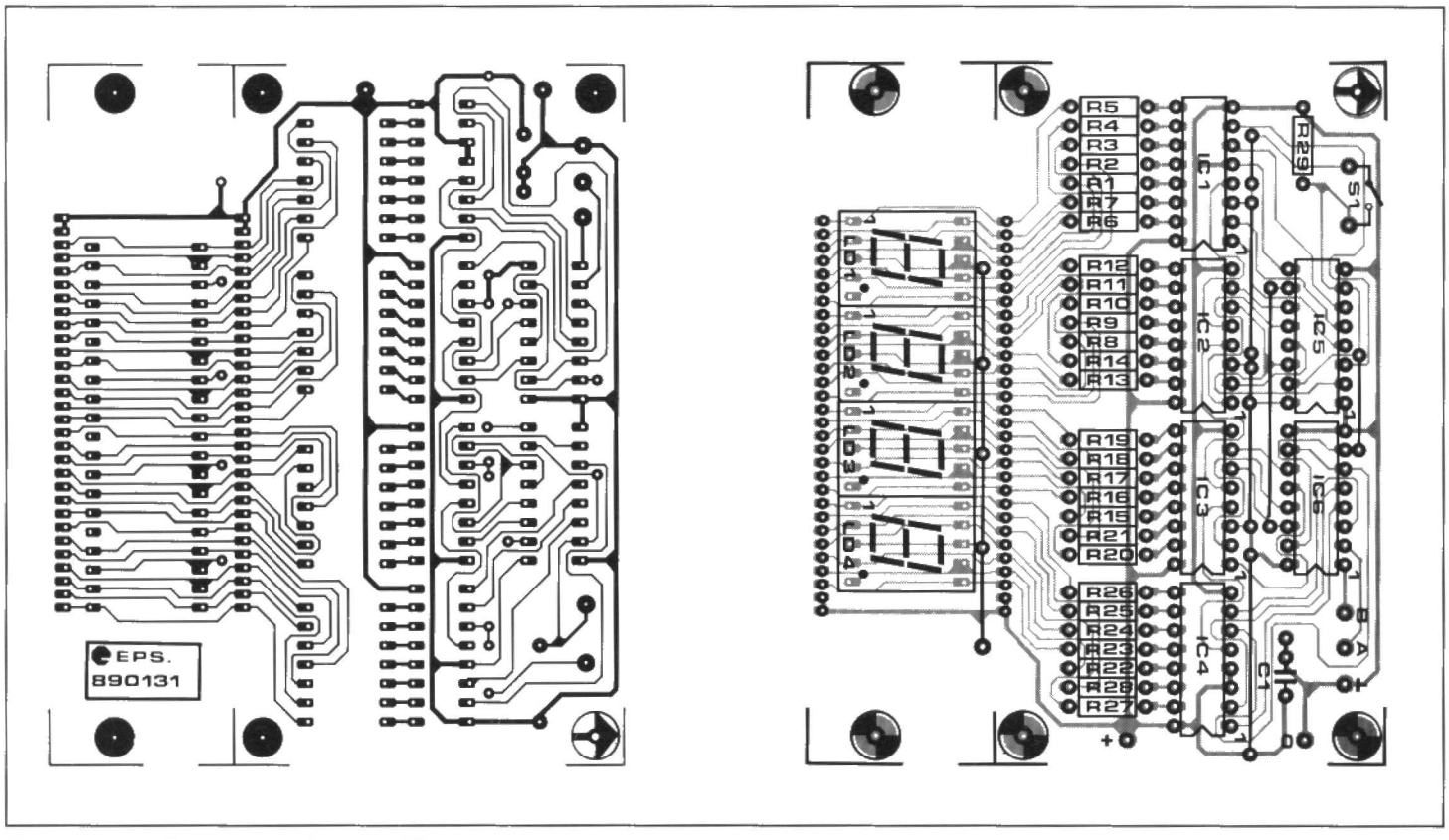


Fig. 3. Printed circuit board for the CD error counter.

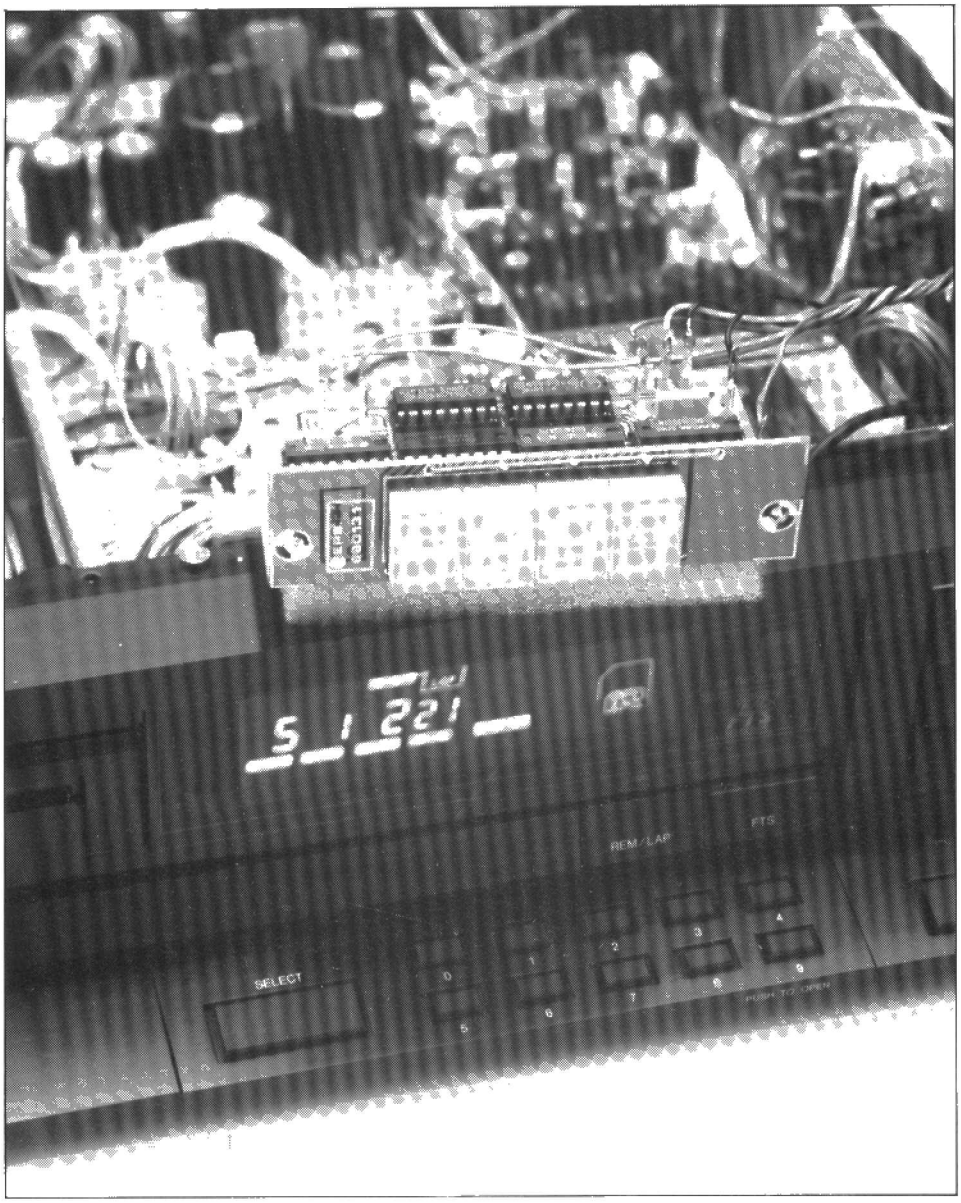
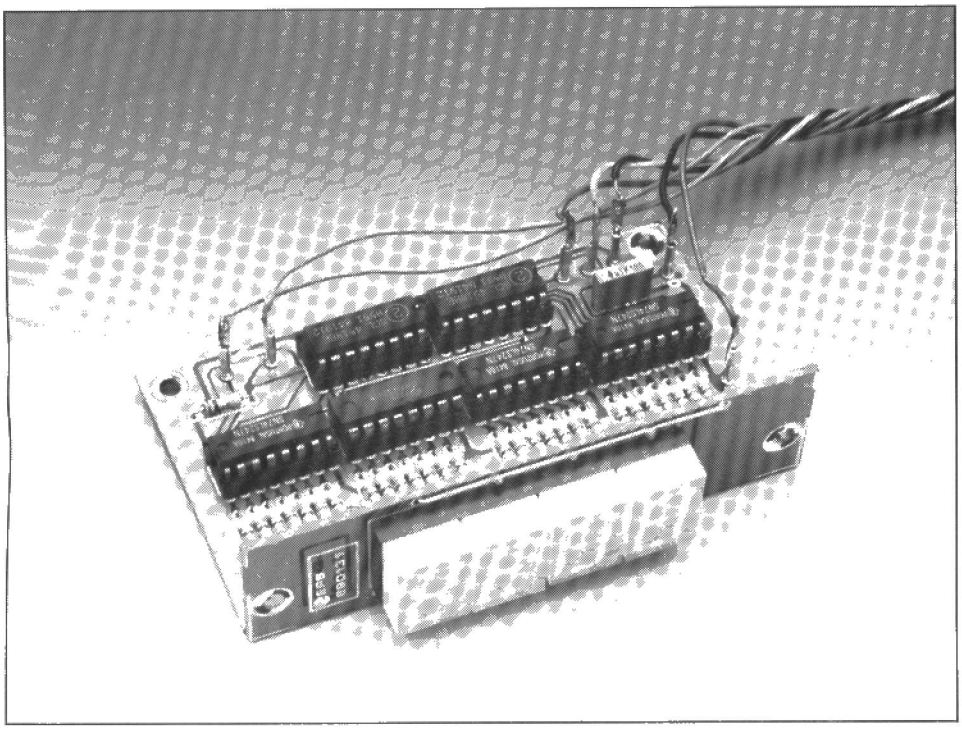


Fig. 4. The prototype circuit connected to a Philips CD960 compact disc player. The display section is mounted vertically on to the main board.



It is also possible to connect the detector to another error signal, EFAB at pin 36 of the SAA7210. EFAB is actuated when the correction and interpolation operations performed by the SAA7210 fail to yield a 100% correct signal, and further interpolation is required by the SAA7220, if fitted. The signal allows you to check whether the information to the D-A converters is a true copy of the original data on the compact disc. If the SAA7220 is called upon for additional interpolation, the CD player makes a 'guess' when it replaces a number of bits found missing. In a practical test, a CD player with good error correction proved capable of producing no EFAB errors in spite of more than 1,000 counted HFD errors.

The 5 V power supply for the circuit must be regulated. If high-efficiency displays are used, it should be possible to power the circuit from the 5 V supply in the CD player. In all other cases, use a standard supply built from a Type 7805 voltage regulator and the usual decoupling capacitors at the input and output.

For further reading:

1. "Decoding ICs for CD players". *Elektor Electronics* January 1989.
2. "Philips-Sony digital audio interface". *Elektor Electronics* June 1988.
3. "Pitch control for CD players". *Elektor Electronics* December 1988.
4. "The compact disc". *Elektor Electronics* July/August 1987.

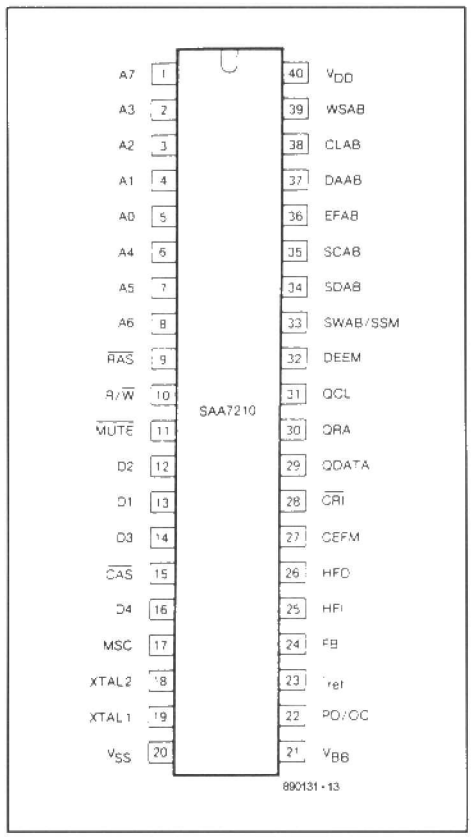


Fig. 5. Pinning of the SAA7210.

RF INDUCTANCE METER

J. Bareford

It is a downright shame not to be able to use many of your inductors simply because their value is not known. First in a new series of budget test equipment for the home constructor, the RF inductance meter leaves coloured bands and unfamiliar codes on high-frequency inductors for what they are, and gives a reliable indication of inductance as well as relative *Q* (quality) factor on an analogue scale. The usable range extends from about 50 nH to 4 mH.

The present inductance meter is intended for high-frequency inductors, and for this reason it is based on a measuring method rather different from that of the digital inductance meter described in Ref. 1.

The principle adopted here is applying a known frequency to an *L*-*C* tuned circuit of which the inductance, *L*, is unknown, and the capacitance, *C*, is variable but calibrated. At a certain value of *C*, the tuned circuit resonates, which is detected by means of a signal rectifier. The value of *C* required to achieve resonance at the known test frequency provides a measure of the inductance, which can be read off as the relative setting of the variable capacitor. The resultant voltage across the *L*-*C* combination provides a measure of the relative loaded *Q* (quality) factor of the inductor under test: the higher the *Q* factor, the higher the resonance voltage.

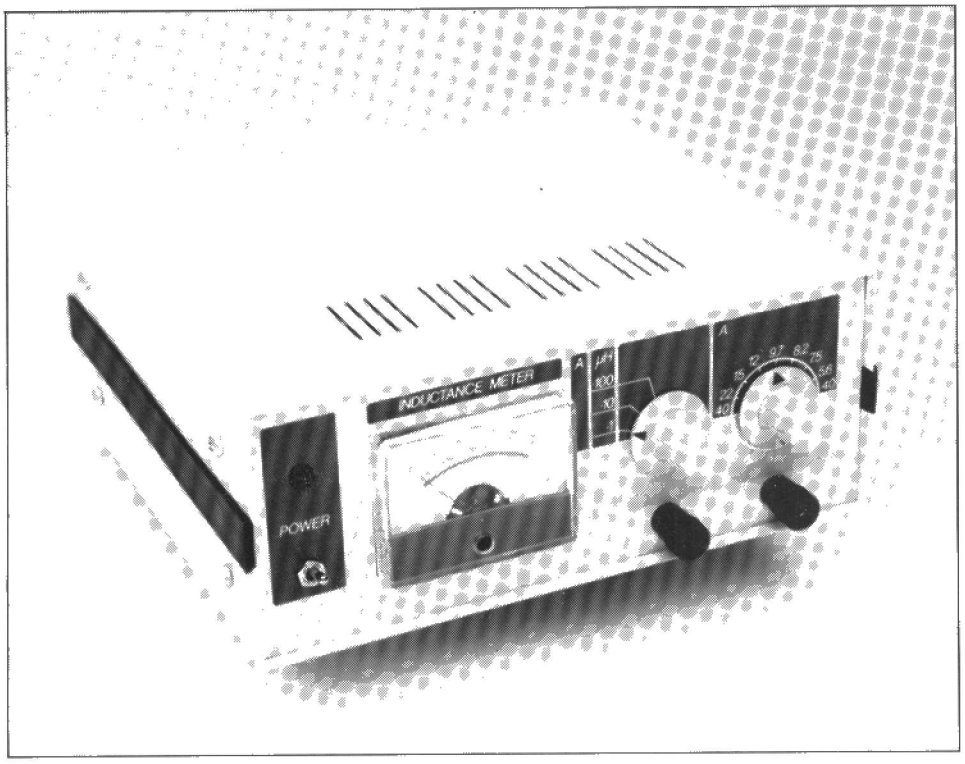
Circuit description

The circuit diagram of Fig. 1 may conveniently be divided into five functional parts.

To begin with, there are two clock oscillators. One, a 7.5 MHz oscillator is set up around quartz crystal X_2 and low-power Schottky inverter N_5. The other, set up around N_1 and X_1, oscillates at 24 MHz, or about $\sqrt{10}$ times 7.5 MHz. The ratio of $\sqrt{10}$ ensures the correct scale factors for the ranges of the instrument.

The second functional part of the circuit is formed by dividers IC_2 and IC_3. Circuit IC_2, a Type 74HCT390 dual decade counter, is driven by the 24 MHz clock signal, and supplies 2.4 MHz (divide-by-10) at output QA1, and 240 kHz (divide-by-100) at output QA2. The second divider, IC_3, is a decade counter Type 74HCT4017. It is driven by the 7.5 MHz clock signal, and supplies 750 kHz (divide-by-10) at the CARRY OUT ($\overline{CO}$) pin.

Five HCMOS bus drivers and associated double *L*-*C* band-pass filters form the third functional block. Impedance matching resistors are fitted between the buffers and the filter inputs. Each band-pass filter is accurately tuned to its input signal frequency to prevent the inductor under test resonating at an harmonic of the test frequency, which would cause too low inductance values to be indicated.



The fourth block is formed by range selector S_1 and wideband push-pull amplifier T_1-T_2. The available ranges and associated multipliers are shown inset in the circuit diagram, and on the front panel of the instrument.

The last functional block consists of the inductor under test, L_x, and the signal rectifier, D_4-C_{34}. The high signal levels used for testing inductors allow a fairly simple rectifier to be used in combination with a common 100 µA moving-coil meter, M_1. L_x is made to resonate with the aid of tuning capacitor C_{33} which is shunted by trimmer C_{32} for calibrating the instrument.

The 5 V regulated power supply around IC_5 is entirely conventional. Permissible unregulated input voltages from a mains adapter lie between 9 V and 12 V. Current consumption is about 190 mA, so that a 250 mA mains adapter may be used.

Construction

Anyone with some experience in electronic construction should be able to build the inductance meter without undue problems. This is mainly by virtue of the double-sided printed-circuit board shown in Fig. 2, which helps to obviate awkward problems with stray inductance, shielding and wires.

The PCB has a large copper surface at the component side to ensure proper screening and decoupling (remember that relatively high signal frequencies are involved). Component terminals inserted in a PCB hole without a white overlay spot are soldered direct to the ground surface at the component side.

Start the construction with fitting the resistors, inductors and diodes. Next, fit the capacitors in the filter sections at the centre of the board. Mount the transistors, trimmer C_{32} (two pitches are allowed; be careful not to overheat the device), and regulator IC_5 (bolt this direct on to the board).

Do not use sockets for the integrated circuits. Study the orientation of the chips, insert them, and solder the following pins direct to the ground plane at the component side:

IC_1: pins 3, 7 and 9;

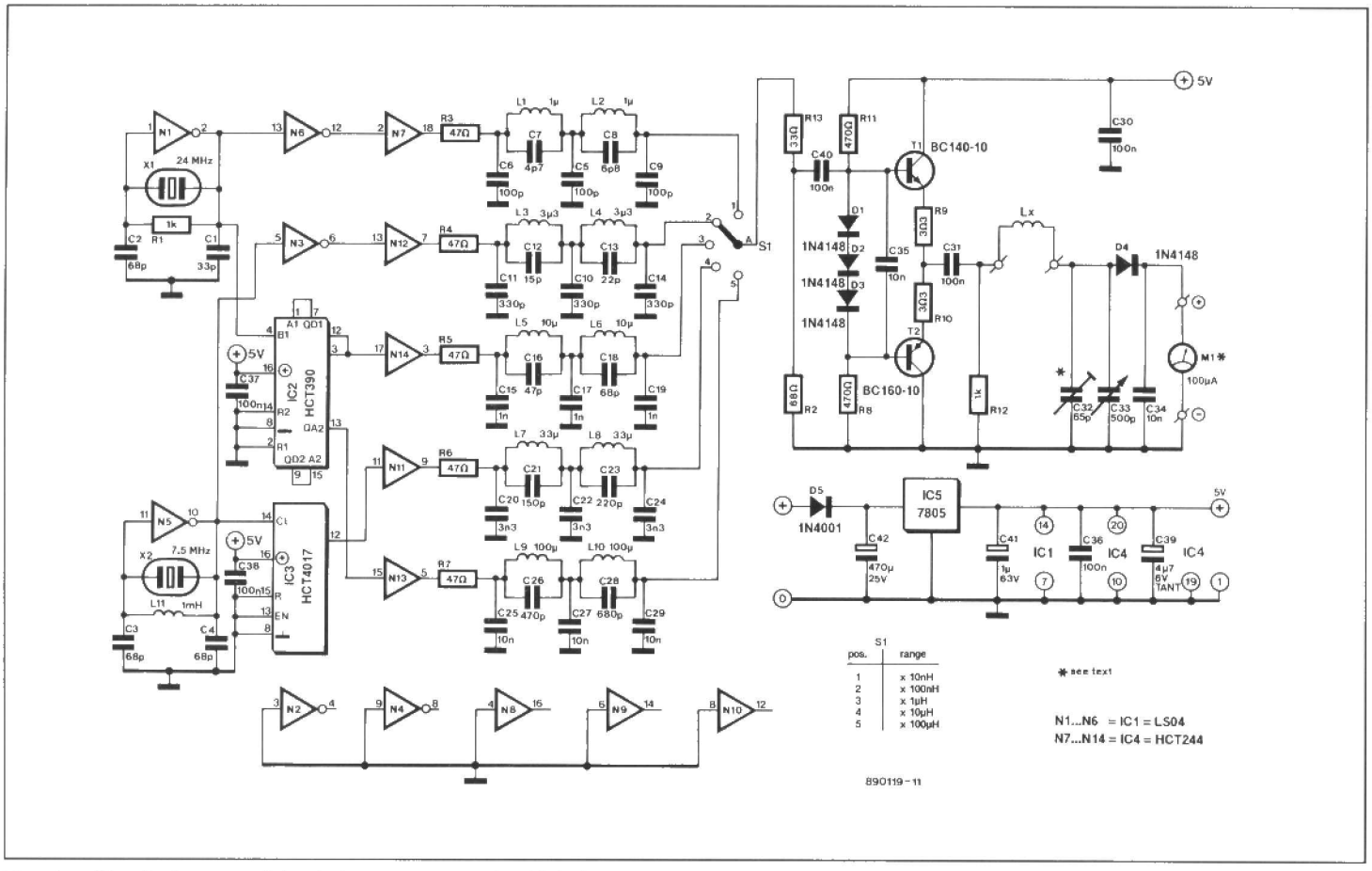


Fig. 1. Circuit diagram of the inductance meter for high-frequency coils.

IC3: pins 13, 11 and 7;
IC2: pins 12, 2, and 7;
IC4: pins 1, 10 and 19.

Then fit the remainder of the components. Do not attempt to solder the enclosures of the quartz crystals to ground, and be sure to use a *PCB-mount* rotary switch — panel-mount types with wires result in too much stray inductance.

The tuning capacitor is a 500 pF mica or PTFE foil type as used in inexpensive MW and SW radios. Mount it at the track side of the board, and use short wires to reach the solder islands (the maximum wire length is about 15 mm). If the tuning capacitor has a separate ground terminal, this must be connected to the grounded solder spot also. The photograph of Fig. 5 shows the completed board.

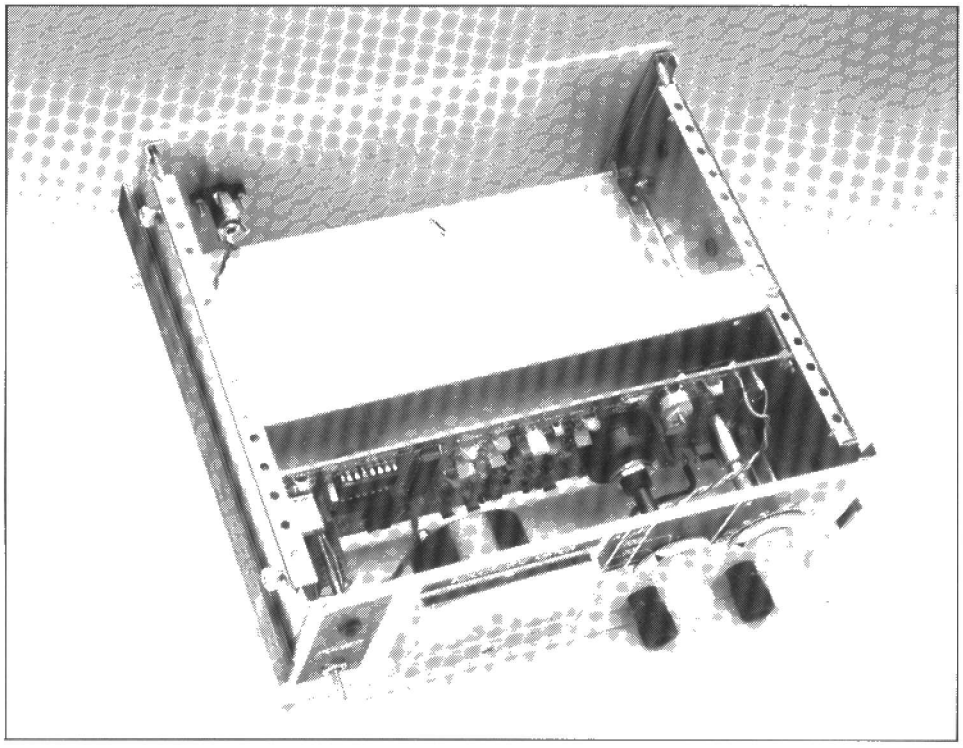
The inductance meter is housed in an ivory white, steel sheet enclosure Type LC850 from Elbomec/Telet. The front and rear panels are made of aluminium. Two side brackets with rows of holes are provided to enable circuit boards mounted in the enclosure to be removed without the need of having to disassemble the box completely.

The front-panel foil for this project is not available ready-made, but its true-size lay-out is given in Fig. 3. Copy the drawing and use it to drill and cut the holes in the front panel of the enclosure. Do not spoil the appearance of the instrument by using the screws provided to secure the aluminium front panel. Instead, use double-sided tape or glue.

Use 20 mm long PCB spacers to mount the completed PCB on to a U-shaped aluminium support bracket (see Fig. 4).

Now fit the moving-coil meter into its front panel clearance, and determine how much space you want to leave between the rear of the meter and the components on the PCB. Insert the support bracket with the PCB on it between the side bars, and shift it forward until the holes in the support bracket align with the holes in the side brackets of the enclosure. Depending on the mounting depth of your panel meter, the fifth or sixth hole from the front of the side brackets should be used. Now mount the front panel and pass the spindles of the range switch and the tuning capacitor through the relevant holes. Determine the length of the spindles required to fit the knobs, and remove the front panel. Use a vice to cut the spindles to the required length.

Mount the POWER LED in a holder. In-



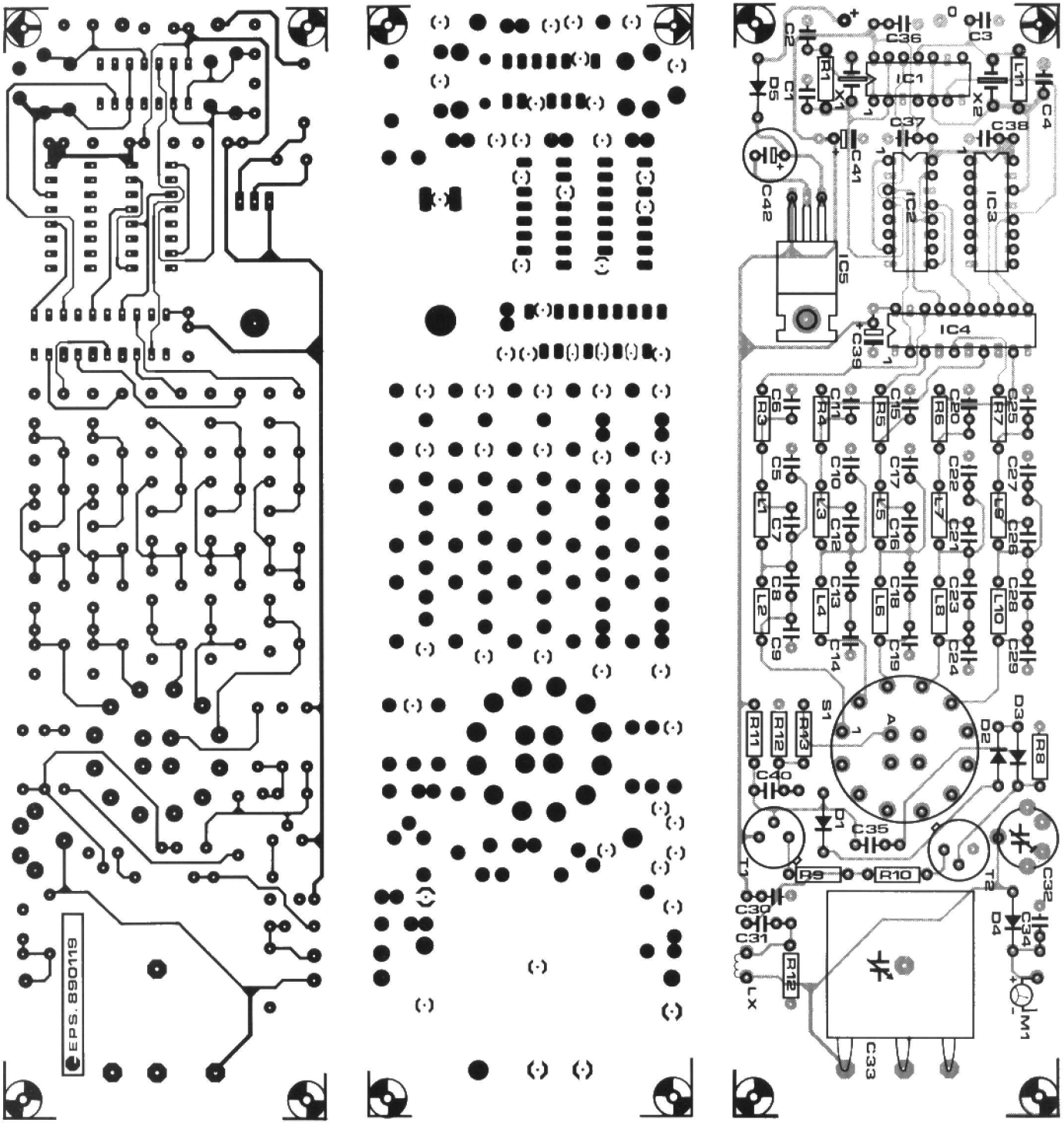


Fig. 2. Track lay-outs and component mounting plan of the double-sided printed-circuit board for the RF inductance meter.

Parts list

Resistors:
R1;R12 = 1k0
R2 = 68Ω
R3–R7 = 47Ω
R8;R11 = 470Ω
R9;R10 = 3Ω3
R13 = 33Ω

Capacitors:

All ceramic capacitors are 5-mm pitch
C1 = 33p ceramic
C2;C3;C4;C18 = 68p ceramic
C5;C6;C9 = 100p ceramic
C7 = 4p7 ceramic
C8 = 6p8 ceramic
C10;C11;C14 = 330p ceramic
C12 = 15p ceramic
C13 = 22p ceramic
C15;C17;C19 = 1n0 ceramic
C16 = 47p ceramic
C20;C22;C24 = 3n3 ceramic
C21 = 150p ceramic
C23 = 220p ceramic
C25;C27;C29 = 10n ceramic
C26 = 470p ceramic
C28 = 680p ceramic
C30;C31;C36;C37;C38;C40 = 100n
C32 = 60p trimmer
C33 = 500p mica-foil tuning capacitor
C34;C35 = 10n
C39 = 4µ7; 6 V; tantalum
C41 = 1µ0; 63 V; radial
C42 = 470µ; 25 V; radial

Semiconductors:
D1–D4=1N4148
D5 = 1N4001
T1 = BC140-10
T2 = BC160-10
IC1 = 74LS04 (do not use HC or HCT versions)
IC2 = 74HCT390
IC3 = 74HCT4017
IC4 = 74HCT244
IC5 = 7805

Inductors:

All inductors are axial types
L1;L2 = 1µH0
L3;L4 = 3µH3
L5;L6 = 10 µH
L7;L8 = 33 µH
L9;L10 = 100 µH
L11 = 1mH0

Miscellaneous:
S1 = 5-way, single-pole rotary switch for PCB mounting.
X1 = 24 MHz quartz crystal (3rd overtone; 30 pF parallel resonance).
X2 = 7.5 MHz quartz crystal (fundamental frequency; 30 pF parallel resonance).
M1 = 100 µA moving-coil meter.
Collet knob with pointer (for range switch).
Collet knob with double pointer (for tuning capacitor).
Solid spindle coupling for tuning capacitor.
Mains adaptor chassis socket.

Enclosure: Telet/Elbomec Type LC850.
Telet srl • Via dell'Intagliatore, 4 • 40138 Bologna • Italy. Telephone: +39 51 534908.
Fax: +39 51 538717.
PCB Type 890119 (see Readers Services page).
Note: we regret that the front-panel foil for this project is not available ready-made through the Readers Services.

stall the ON/OFF switch and the two black, insulated wander sockets on to the front panel, then wire these components. The wires between the wander sockets and the PCB terminals marked Lx must be relatively thick, and as short as possible. Do not twist them!

The final assembly and the connecting of wires to the terminal posts on the PCB is straightforward. The rear panel is drilled to accept a mains adaptor socket as

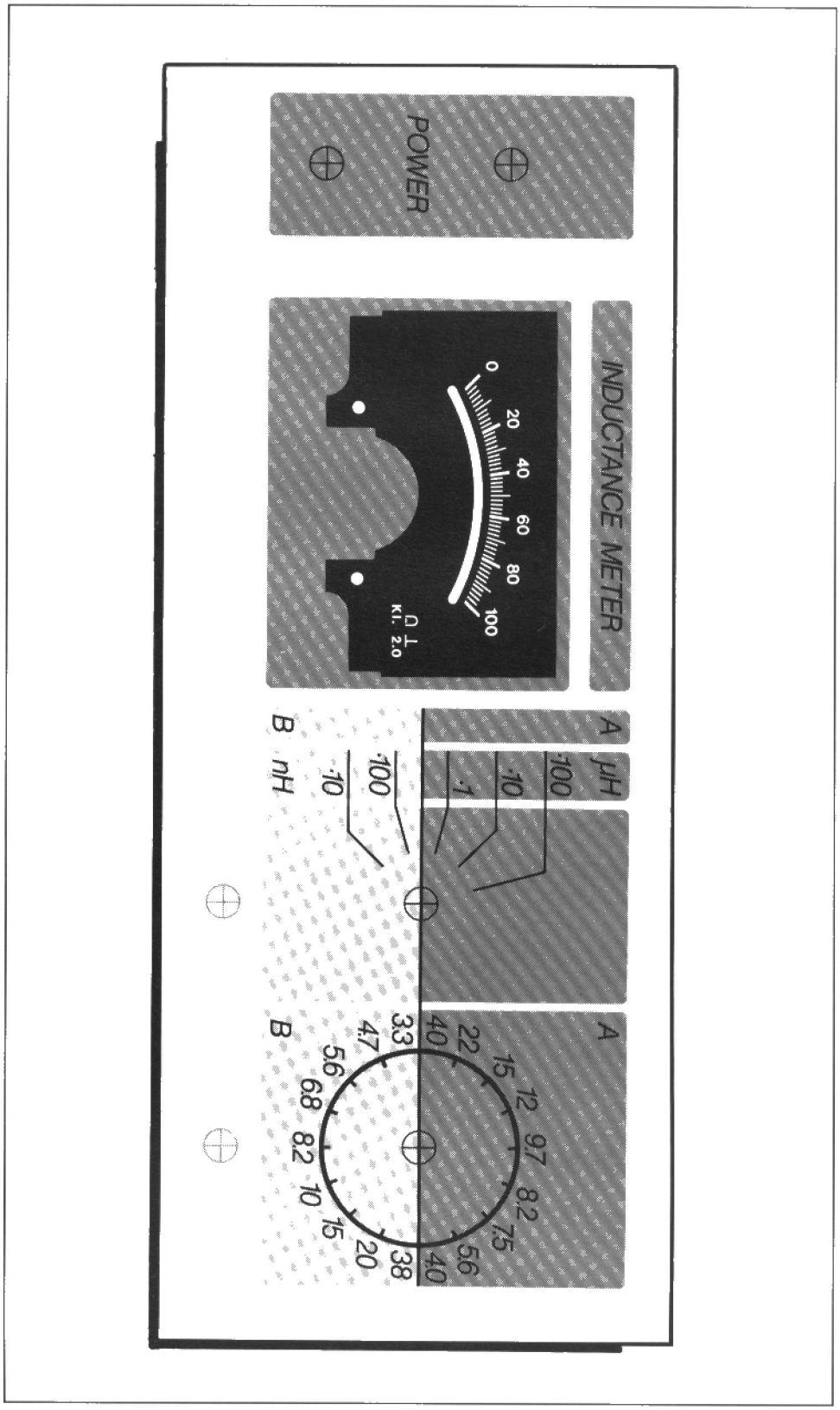


Fig. 3. The front-panel. If possible, the areas marked 'A' should be given a different colour from areas marked 'B' to avoid confusion in the use of the two scales.

used on portable cassette recorders and calculators. Be sure to observe correct polarity!

Practical use

Any inductance measurement must start in the range for the highest inductance values (range switch position 5 in the circuit diagram), i.e., using the lowest test frequency. Do not switch up from the low-value ranges to the high-value ranges — this is likely to cause false readings owing to the inductor resonating at a harmonic frequency.

Start in the ×100 µH range, and turn C_{33} until the meter deflects. Switch to a lower range if the meter does not deflect. Operate C_{33} again until a sharp peak is observed.

The first three ranges, ×100 µH, ×10 µH and ×1 µH, use scale 'A' (4.0–40) of the tuning control. The next range, ×100 nH, uses scale 'B' (3.3–38). The lowest range, ×10 nH, is only suitable for comparative inductance measurements, since the internal capacitance and inductance of the instrument are significant at 24 MHz. The calibration of the lower half of scale 'B' is, therefore, unlikely to be valid for accurate measurements, but still allows comparative tests to be carried out on batches of inductors. Similarly, the maximum meter indication provides a relative, not an absolute, indication of the Q factor in all ranges.

Calibration

The meter is fairly simple to calibrate. Connect an inductor whose value is accurately known. If you are unable to obtain a reference inductor, use a ready-made choke with a tolerance of 5% (e.g., Cirkit's FL4 series). A value near the maximum indication within a range must be chosen, so that the tuning capacitor is set to minimum capacitance. This ensures the largest effect of the parallel capacitance formed by trimmer C_{32}. Connect a choke of 220 µH or 390 µH (scale 'A', range ×10 µH), and set the tuning capacitor as accurately as possible to indication '22' or '40' respectively. Carefully adjust trimmer C_{32} for maximum meter deflection. Connect other, but similarly selected, inductors, and repeat the adjustment for the three highest ranges until an acceptable compromise is reached as regards accuracy of the scale. It should be noted that the resolution and repeatability so achieved depend on the accuracy at which the tuning scale has been reproduced.

Finally, some moving-coil meters have such a low internal resistance as to require an external series resistance to be fitted to prevent the needle hitting the right end of the scale when a high-Q inductor is being tested. The value of the series resistor, if required, must be determined experimentally.

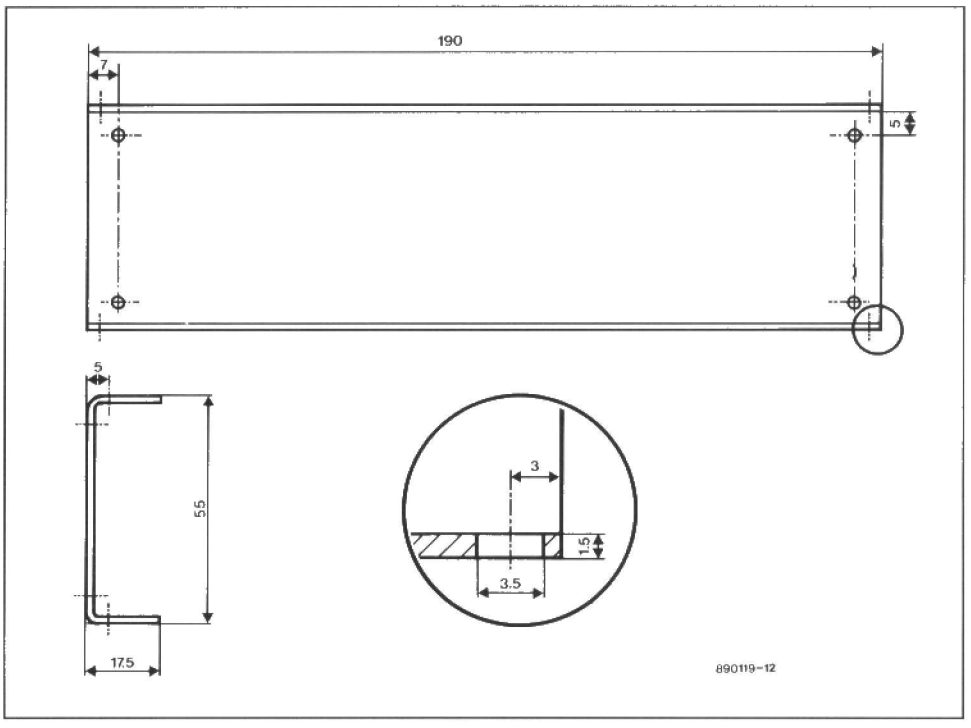


Fig. 4. Construction details of the aluminium bracket that holds the PCB.

Reference:

1. "Self-inductance meter". *Elektor Electronics* September 1988.

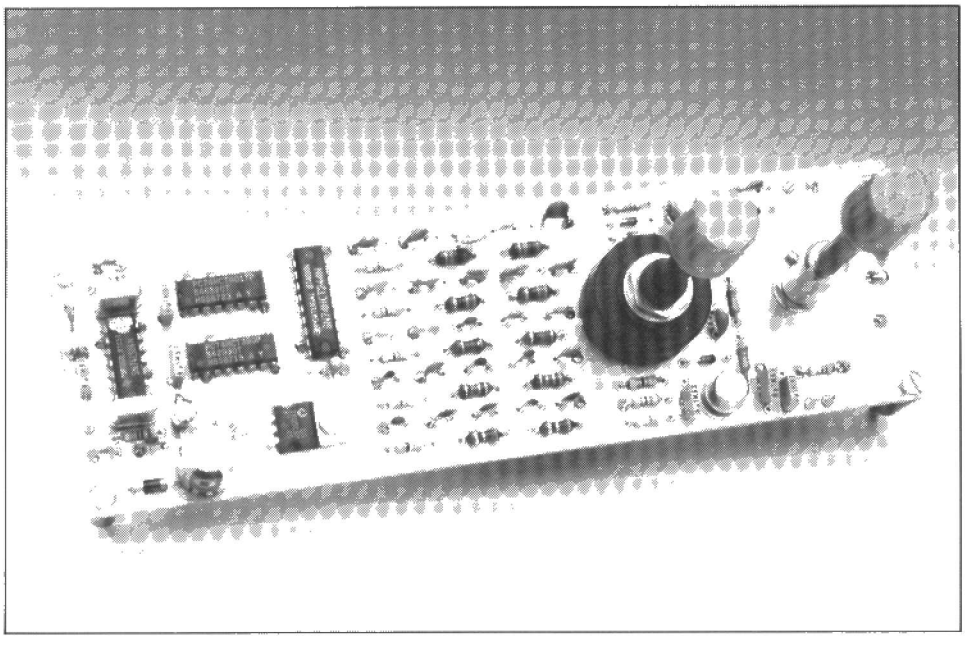


Fig. 5. Completed PCB before installation in the enclosure. Note that a dual-pointer knob is fitted on the spindle of the tuning capacitor.

THE DIGITAL MODEL TRAIN – PART 7

by T. Wigmore

The seventh part in the series deals with the circuit description of the main unit in the Elektor Electronics Digital Train System. The construction and testing will be the subject of next month's instalment.

The main unit consists essentially of a single-board processor system based on a Z80 as shown in Fig. 47. This processor was chosen not only for its very low price, but also because the special Z80 peripheral chips (PIO – parallel input/output – and CTC – counter timer control) make it possible to use the powerful Z80 interrupt structure without the need of additional logic. Since the train system requires a number of asynchronous processes to be carried out more or less simultaneously, this is a very worthwhile aspect.

Apart from the standard Z80 design, consisting of the processor proper, memories and a CTC for general timing functions, the unit also contains various I/O structures.

Reading of the locomotive controls is carried out by an analogue-to-digital (A-D) converter that has 16 multiplexed analogue inputs. The results of the A-D conversions and the position of the function switches associated with the locomotive controls are read via a PIO port. Set locomotive addresses are read on to a separate bus via a diode matrix. This matrix may be considered a primitive 16-byte manual access memory (MAM), which has the advantage that no knowledge of programming is required to set the addresses. The setting may be carried out with the aid of diodes, DIL (dual-in-line) switches or thumbwheel switches.

Main features

- independent control of up to 81 locomotives
- accepts up to 16 manual controls
- on-board locomotive addressing
- controls up to 324 turnouts (points) and signals (648 solenoids)
- manual control of turnouts (points) via keyboards
- stand-alone or computer-controlled operation via RS232 interface
- integral interface for monitoring signals via the track
- compatible with Märklin Digital
- low-cost Z80 microprocessor; 2.45 MHz, 8 K ROM; 8 K RAM
- excellent price/performance ratio

The keyboards are connected to the Z80 bus via a 20-way connector and the keyboard interface. The 20-way connector indicates that, in contrast to the Märklin system, the keyboards are driven in parallel. Märklin's serial keyboard drive requires a microprocessor for each keyboard. Since our keyboards do not need a microprocessor, the relevant circuits have remained fairly simple. The cost of this is, of course, a 20-way connector between the main unit and the keyboards but, since keyboards are normally located next to the main unit anyway, that is hardly a disadvantage.

The main unit also has a serial output to the booster. The serial signals (binary coded trinary data) are generated by a special function IC. One timer of the CTC is used as the clock for the serial-signal generator, so that the baud rate may be adjusted with the aid of software. This is necessary, because switching instructions for signals and turnouts (points) need to be sent at higher speeds than the locomotive control commands.

Finally, there is a bi-directional serial (semi duplex) RS232 interface, but this does not make it necessary for the train system to be controlled via a computer: the unit is perfectly suitable for stand-alone operation. However, the RS232 interface makes the system considerably more versatile.

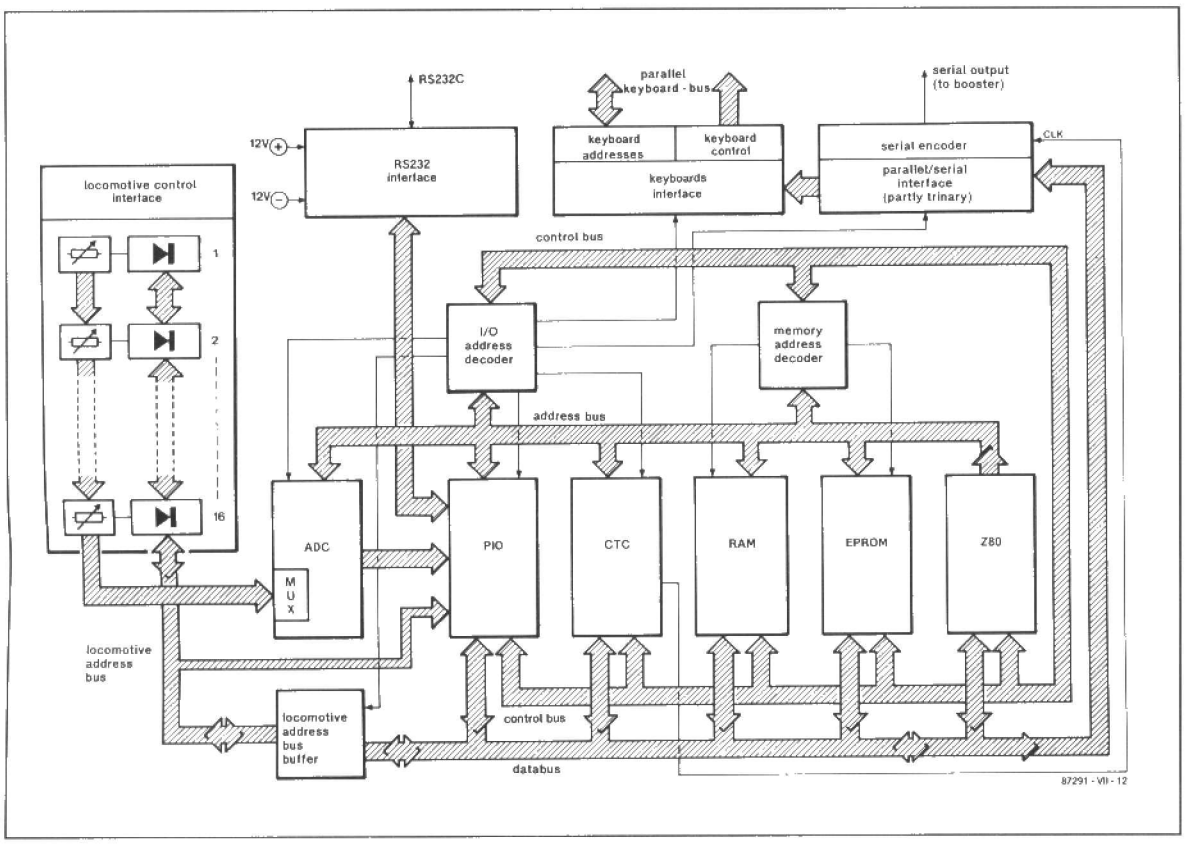


Fig. 47. Block schematic of the main unit, which is essentially a Z80-controlled single-board computer

Circuit diagram

The 5-V supply at the top left in the circuit diagram of Fig. 48 is a standard design, except for D36. This diode ensures that the current through the keyboard

LEDs (taken from V++ via K19) does not load smoothing capacitor C25. This is necessary, because this current may be quite substantial (several amperes) if a large number of keyboards is used. This is also the reason that D38–D41 are heavy-duty types.

The supply for the RS232 drivers in IC10 is provided by IC15 and IC16. These components are necessary even if the RS232 interface is not used, because two gates in IC10, N2 and N5, are used for driving the booster. The input voltages for IC15 and IC16 (+20 V and –20 V respectively) are derived from the booster circuit.

The serial control data are encoded by IC27. Inputs D1–D4 are driven via electronic switches ES1–ES4. These four bits form the address section of the control data and are defined in three-state logic, that is, they are '1', '0' or 'undecided'.

The data section, D5–D9, functions with binary logic and is, therefore, connected direct to the outputs of IC17. Output latches IC17 and IC23 ensure that the serial data remain stable during transmission. As soon as the address part of a data byte is placed into IC23, the start instruction for serial transmission ($\overline{TE}$) is given via N6.

The clock for IC27 is derived from the second timer in the CTC, IC12, to enable the speed of the serial transmission via the software. The clock is divided by two in FF3 to obtain a 50% duty factor, which is necessary for the correct operation of IC27.

The clock pulses to IC27 are counted by the CTC. After 200 pulses, a data byte is transmitted twice and an interrupt is generated. The interrupt routine prepares the next data byte to be transmitted and starts the next transmission cycle.

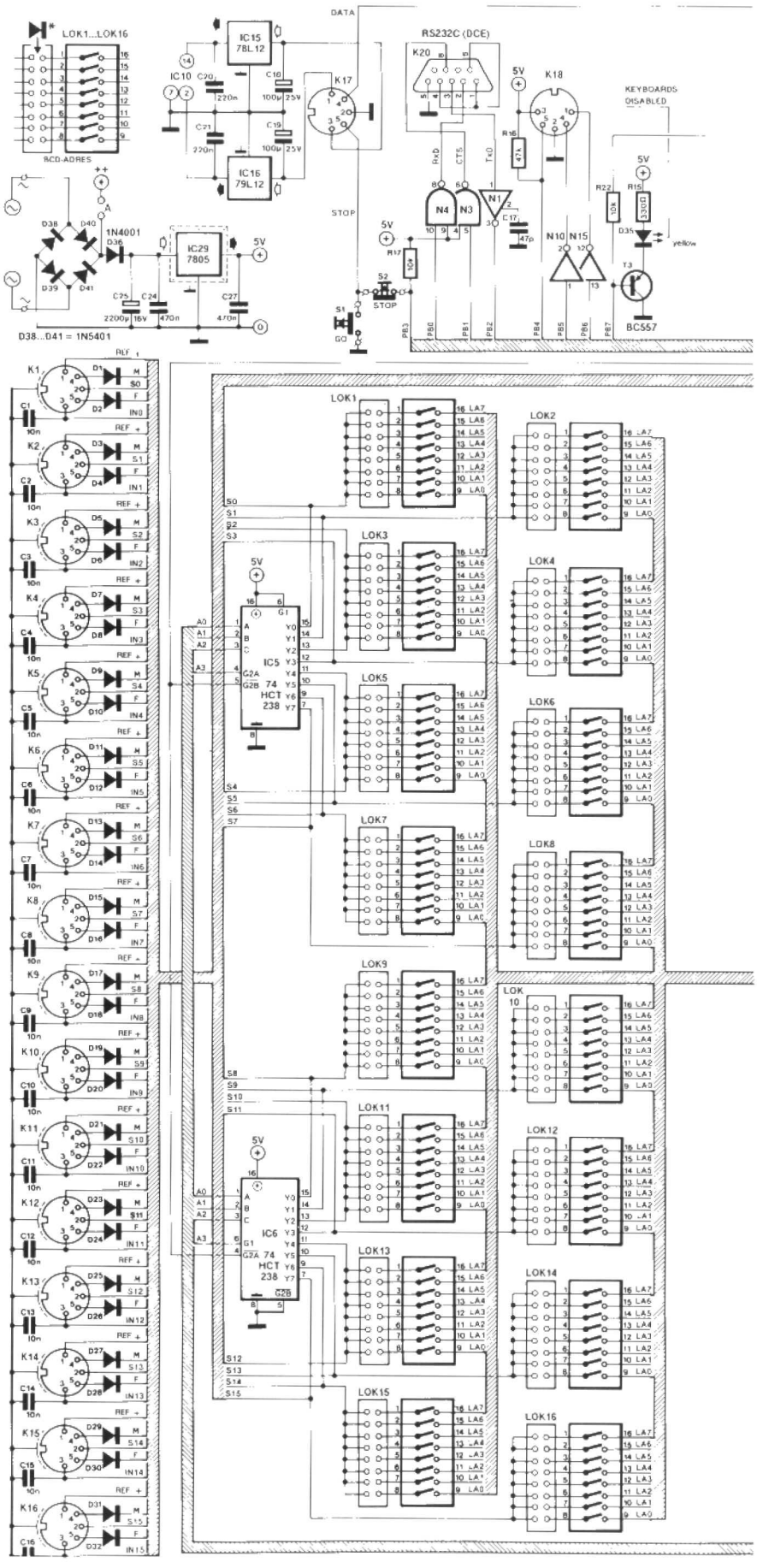
The output signal of IC27, which swings between 0 V and 5 V is amplified and made symmetric (±12 V) by N5. Since the signal is inverted by this gate, it is inverted again by N2 and then passed to the booster via Re1 and K17.

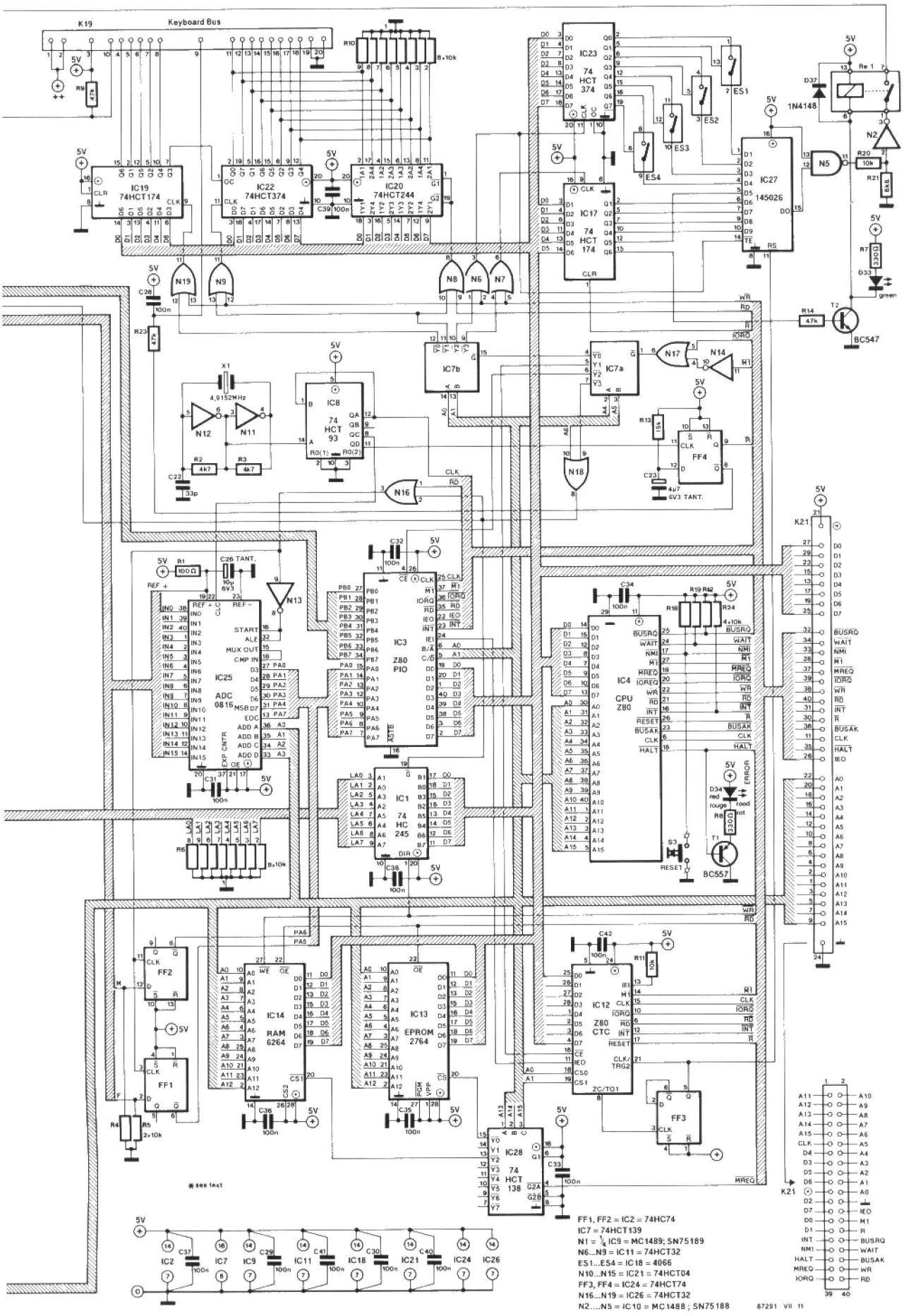
Output Q6 of IC17 is used to drive relay Re1. When the relay is not energized, the output of the unit, and that of the booster, is high-impedance, so that no voltage is applied to the track.

The oscillator, N11-N12, is followed by binary scaler IC8, whose output QA delivers the 2.45 MHz system clock. This frequency was chosen, because it enables both the baud rate of the RS232 interface and the various frequencies for the serial transmitter to be derived from it. Output QC provides a 614 kHz signal that is used as the clock for the A-D converter.

The circuit around the CPU (central processing unit), IC4, the PIO, IC3, and the CTC, IC12, is entirely standard and will not be discussed here.

The address decoding for the memories is carried out by IC28. This circuit splits the addressable memory locations of up to 64 kbyte into eight pages of 8 kbyte each. Page 0 (0000–1FFFH) contains the control program for the system, which is available as an EPROM, coded ESS572 (see the Readers services page towards the back of





FF1, FF2 = IC2 = 74HC74
IC7 = 74HCT139
N1 = ¼ IC9 = MC1489; SN75189
N6...N9 = IC11 = 74HCT32
ES1...ES4 = IC18 = 4066
N10...N15 = IC21 = 74HCT04
FF3, FF4 = IC24 = 74HCT74
N16...N19 = IC26 = 74HCT32
N2....N5 = IC10 = MC1488 ; SN75188

87291 VII 11

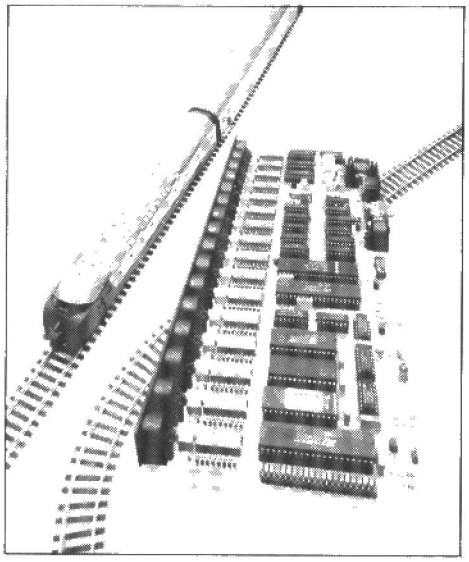
Fig. 48. Circuit diagram of the main unit of the Elektor Electronics Digital Train System

this issue. The EPROM contains unallocated space that may be used for any future extensions of the program.

The RAM is contained on page 2 (4000H –5FFFH) and this page is also largely unused. The system uses 2 kbyte, a further 2 kbyte is reserved for possible future extensions and 4 kbyte is available for downloading of user programs that are actuated via special RS232 commands. Table 5 shows the memory mapping.

The I/O addresses that are available on outputs A0–A7 of the CPU during read or write instructions are decoded by IC7. Here again, some space is not used and 32 I/O addresses are reserved for possible future extensions. See also Table 6.

The locomotive addressing is carried out via IC5 and IC6. Up to 16 selections may be made: S0–S15. If a selection signal is made active, that is, '1', the relevant lines LA0–LA7 (LA= locomotive address) that are connected to the selection line via a diode will also go high. Lines without a diode are held low ('0') by a pull-down resistor (contained in array R6).



The locomotive addresses, which are in BCD (binary-coded decimal) format, are read via buffer IC1. The reason that IC1 is a bidirectional buffer although the locomotive addresses can only be **read** by the diode matrix is that in future a select-and-display board may be used for the locomotive addressing.

At the relevant locomotive control, the address is set via the RS232 interface and written to the display board via IC1. This ensures that the display at all times shows to what address a given control is set. The practical implementation of the diode matrix will be described in next month's instalment.

At the same time the locomotive address is read, the position of the function controls is read into bistables FF1 and FF2, one of the 16 analogue inputs of the A–D converter is selected and a conversion is started. The analogue input, address at A0–A3, is taken to the converter via the address-latch-enable signal at pin 32. The conversion start signal is available at pin 16.

When the end-of-conversion signal (EOC at pin 13) becomes active, the converted signal is applied to the PIO. Five bits are used: four for the speed and one for the direction. The remaining two inputs of gate A of the PIO, PA5 and PA6, are used to read the position of the function switches.

Gate B of the PIO is used for the start/stop line (also the booster overload signal line), the interface for the monitors and the RS232 interface. The output lines are buffered.

Gates N10 and N15 ensure the provision of adequate current to the (relatively) capacitive load presented by the monitor bus.

Gates N3 and N4 adapt the logic 0–5 V level to the ±12 V RS232 level. Gate N1 does the opposite for incoming RS232 signals.

Control of the RS232 is entirely via software and will be dealt with in detail in a forthcoming article in this series.

Integral test program

Testing of the board is facilitated by the test routines incorporated in the system program. The most important of these is the service loop. This is actuated when the power is switched on while the GO switch is (kept) depressed. As long as S1 is closed, the service loop will remain active. During sustained testing it is, therefore, advisable to short-circuit the switch.

The service routine places VLF (very low frequency) square wave signals on the various output ports. These signals may be checked with a multimeter. Also, a yellow LED (D35) flashes in a 1 Hz rhythm and the LEDs on the keyboards will be driven sequentially. The service routine is disabled by opening S1.

If the booster was connected (which is not required during service checks), it may be necessary to press stop key S2 briefly to actuate the service loop.

A standard multimeter (analogue: R_i = 20 kΩ/V or digital) and an oscilloscope or frequency meter are required for testing and checking. If an oscilloscope or frequency meter is not available, not all recommended test can be carried out, which results in a somewhat greater uncertainty factor. However, if the construction has been carried out carefully, there is not much risk of anything going wrong, particularly not since the circuit has no calibration points whatsoever.

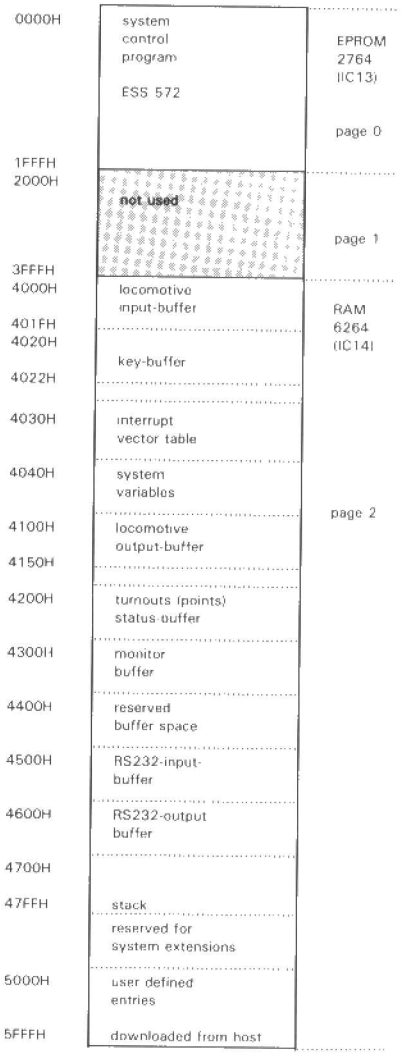


Table 5. Memory mapping

I/O-address		I/O-device	
binary	HEX		
XX00XX00	C0H	drive	keyboard
XX00XX01	C1H	address bus	
XX00XX10	C2H	adress section	serial encoder IIC27I
XX00XX11	C3H	data section	
XX01XX00	D0H	counter/ timer 0	CTC
XX01XX01	D1H	counter/ timer 1	
XX01XX10	D2H	counter/ timer 2	
XX01XX11	D3H	counter/ timer 3	
XX10XX00	E0H	gate A data	PIO
XX10XX01	E1H	gate A control	
XX10XX10	E2H	gate B data	
XX10XX11	E3H	gate B control	
X0110000	B0H	locomotive address bus & ADC multiplexer	
X0111111	BFH		
01110000	B0H		
01111111	BFH	spare	
11110000	F0H	I/O-addresses	
11111111	FFH		

X = don't care

Table 6. Input/output mapping

APPLICATION NOTES

The content of this column is based on information obtained from manufacturers in the electronics or allied industries, or their representatives, and does not imply practical experience by *Elektor Electronics* or its consultants

LOG/ANTILOG AMPLIFIER TYPE SSM-2100

The SSM-2100 from Solid State Microtechnology, a Precision Monolithics Inc. (PMI) company, is a complete monolithic subsystem for the realization of logarithmic and exponential transfer characteristics. It contains two precision opamps, a high conformance transistor pair, a precision bandgap voltage reference and a substrate temperature regulator that stabilizes the scale factor and greatly attenuates drift of the reference. A negative reference voltage is also available to facilitate external trimming.

Features

- 500 pA input bias current (untrimmed)
- 50 pA input bias current (trimmed)
- 4 mV input offset voltage
- 10 ppm/°C reference drift
- 30 ppm/°C scale factor drift
- 0.25% conformance
- 3 decade dynamic range (voltage input)
- 5 decade dynamic range (current input)

Applications

- Photodiode preamplifier
- Absorption measurement
- Log sweep generators
- High resolution data acquisition
- Analogue computation circuits
- Analogue compression/expansion
- Linear-to-dB conversion

Inputs

Like all log amplifiers, the SSM-2100 has a limited dynamic range for voltage inputs, owing partially to the input offset voltage (which can be trimmed). Therefore, for widest dynamic range, current inputs are recommended. Since most wide-range transducer inputs (such as photodiodes) closely resemble current inputs, this is not usually a problem. Untrimmed, the 2100 can handle about 5 decades of dynamic range in log mode or about 10 decades in log ratio mode. When trimmed, this may be extended to at least 6 decades (12 decades in log ratio mode).

The application circuits in this article are, for convenience, shown for voltage inputs, although all configurations may be used for current inputs, in which case R_{IN} can be omitted. To ensure unconditional stability, however, it is recommended that the input be shunted to ground with a 10 kΩ resistor in series with a 10 nF capacitor when a true current input is used.

Negative supply

The negative supply is internally regulated at –7 V. A current-limiting resistor, R_{LIMIT}, is required in series with pin 7. For most applications, a value of 1.6 kΩ for –15 V supplies is recommended. The voltage at pin 7 is thus quite stable and is useful when the unit is trimmed

SPECIFICATIONS* — **OPERATING TEMPERATURE** –10°C to +55°C — **STORAGE TEMPERATURE** –55°C to +125°C

The following specifications apply for V_s = ±15V, R_{LIMIT} = 1.6kΩ, 5°C ≤ T_A ≤ 50°C, I_{REF} = 1mA, unless otherwise noted.

PARAMETER (SYMBOL)	MIN	TYP	MAX	UNITS	CONDITIONS
Conformity Error[1] (V_{ERROR}) (Note 1)		0.25		%	I_{IN} = 100nA to 100µA
		0.4		%	I_{IN} = 10nA to 1mA (Input Offset Trimmed)
Scale Factor (V_{SCALE})	65	70	75	mV/Decade	Measured at Pin 16
Scale Factor Temperature Drift (TC V_{SCALE})		30		ppm/°C	
Input Offset Voltage (V_{OS}) (Note 2)		4	8	mV	
Input Bias Current (I_B) (Notes 1, 2)		500	2000	pA	
Output Offset Voltage (V_{OOS})		30	70	mV	I_{IN} = I_{REF} 1mA Scale Factor Set at 1V/Decade
Power Supply Rejection Ratio (PSRR) (Note 3)		500 250		µV/V µV/V	+12V ≤ V+ ≤ +17V –12V ≥ V– ≥ –17V Scale Factor Set at 1V/Decade
Output Voltage Swing (V_{OUT})	–11 –10.2		–10 +10	V V	R_L ≥ 10K R_L ≥ 2K
Reference Output Voltage (V_{REF} +)	4.7	5.0	5.2	V	No Load
Reference Output Voltage Temperature Coefficient (TC V_{REF})		10		ppm/°C	
Reference Output Current	5			mA	
Reference Load Regulation		0.015		%/mA	R_L ≥ 1KΩ
Reference Supply Rejection		0.04		%/V	+12V ≤ V+ ≤ +17V
Voltage at Pin 7 (V_{REF} –)	6	7	8	V	
Positive Supply Current (I_S +)		35 20 50 5		mA mA mA mA	T_A = 25°C T_A = 50°C T_A = 5°C Heater Disabled
Negative Supply Current (I_S –)		5		mA	
Heater Start up Current		80	120	mA	
Regulated Chip Temperature (T_{REG})	53	60	75	°C	

Notes
1). Guaranteed by design but not directly measured.
2). Applies to both signal and reference inputs
3). Referred to output in log mode, or to input in antilog mode
4). Specifications apply after a 50 second warmup period.

*Final specifications may be subject to change

Power supply decoupling and earthing

Because of the high gain of the temperature regulator circuit, generous positive supply decoupling should be used. The 0.2 µF decoupling capacitor shown on the application circuits should be of a ceramic type and mounted as close to pins 1 and 4 as possible. An additional capacitor of about 50 µF or more should also be included on the board. It should also be noted that pin 1 carries all the heater current, and care should be taken when laying out earth lines to prevent this from causing errors. The negative supply is internally regulated and needs no decoupling.

Temperature control

The internal chip temperature is regulated at about 60 °C, but this can be adjusted via pin 2. To decrease the temperature by n °C, a resistor of value $3.5/n$ MΩ should be connected between pins 2 and 10. To increase the temperature by n °C, a resistor of value $6/n$ Ω should be connected between pins 2 and 7. The regulator can be shut off completely with a 100 kΩ resistor from pin 2 to +V. This is useful in low power applications. With no regulation, the reference drift is about 70 ppm/°C, and the scale factor drift about –3300 ppm/°C. The latter can be compensated by the use of a temperature compensating resistor instead of R2.

Inverting log amplifier

Figure 1 shows the 2100 used in the inverting log mode. With Iin = Iref (Vin = 10 V with values shown), the output will be zero, and will increase at 1 V/decade as Iin reduces. The 10 V input range optimizes dynamic range in +15 V systems, but can be changed proportionally by adjusting Rin. Adjusting R1 will alter the scale factor, while adjustment of Rref will alter the output offset at a given Vin.

Capacitors C1, C2 and C3 provide phase compensation for the system, yielding a 30 kHz small signal bandwidth at Iin =1 mA, 8 kHz at Iin = 1 µA, and 1.6 kHz at Iin = 100 nA. This can be improved by a factor 3 by increasing C2 to 10 nF and reducing C1 to 2 nF at the expense of some peaking at the upper range of input current.

Non-inverting log amplifier

Interchanging the signal and reference inputs results in a non-inverting log amplifier as shown in Fig. 2. In this case, the output crosses zero with the input five decades below full scale, but this can be altered by adjusting R3. A slight inaccuracy is caused by R1 and R2 adding to the base resistance of the logging transistors, but this is minimized by keeping these as small as possible.

The small-signal bandwidth is 5 kHz with Iin from 1 µA to 1 mA and is better than 2 kHz over the full five decade range.

Log ratio applications

The 210 is well suited to log ratio applications where the output is proportional to the logarithm of the ratio of two input currents or voltages. This is because both the signal and reference inputs operate at true virtual earth eliminating the need of a true current found in other configurations.

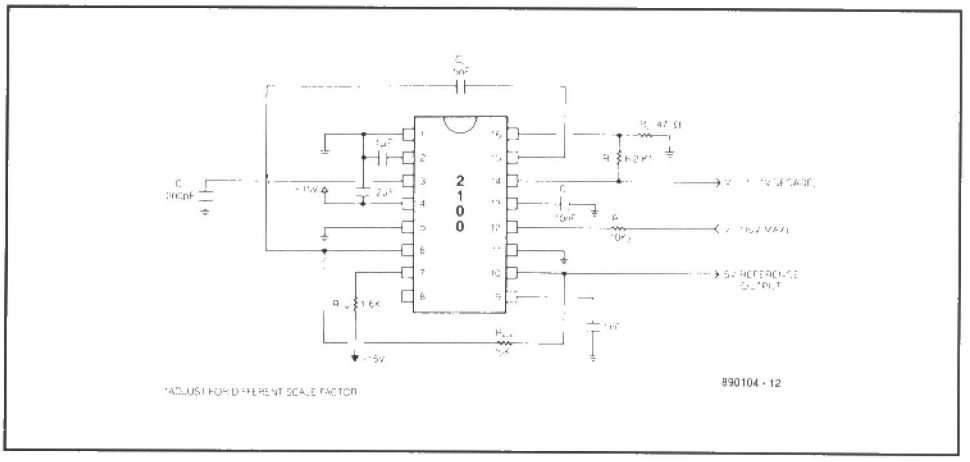


Fig. 1. Inverting logarithmic amplifier

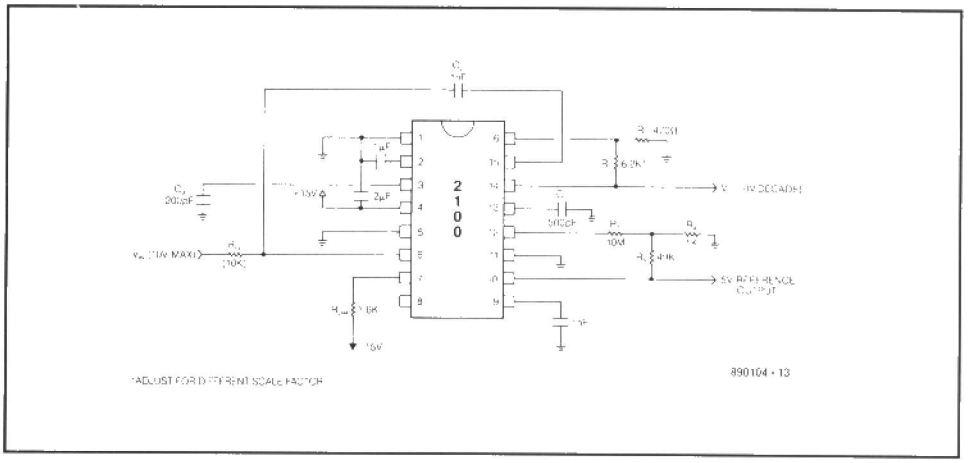


Fig. 2. Non-inverting logarithmic amplifier

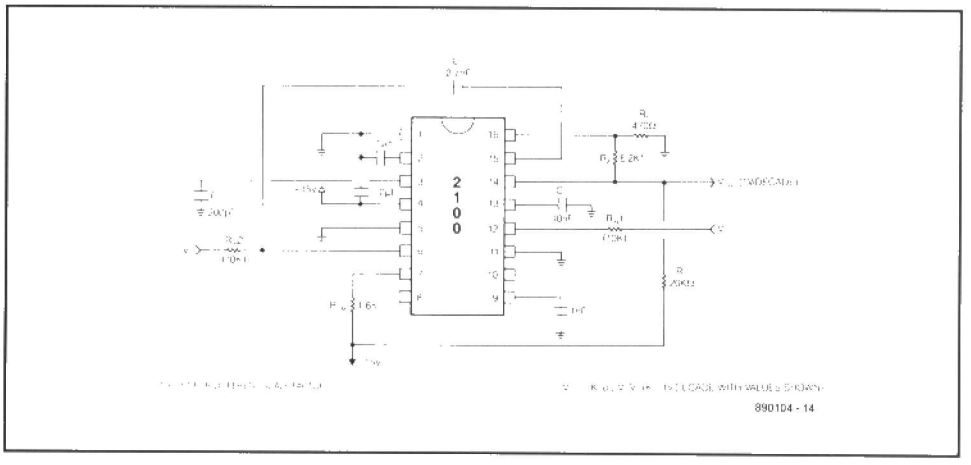


Fig. 3. Logarithmic ratio amplifier

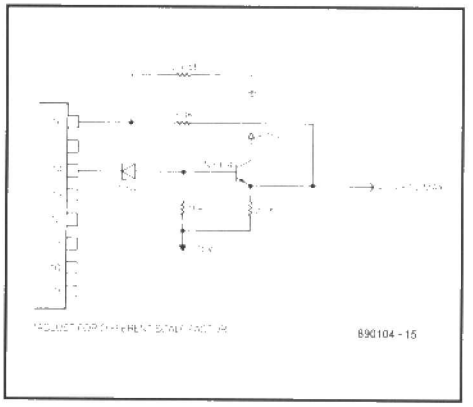


Fig. 4. Modification to Fig. 3 for four quadrant operation

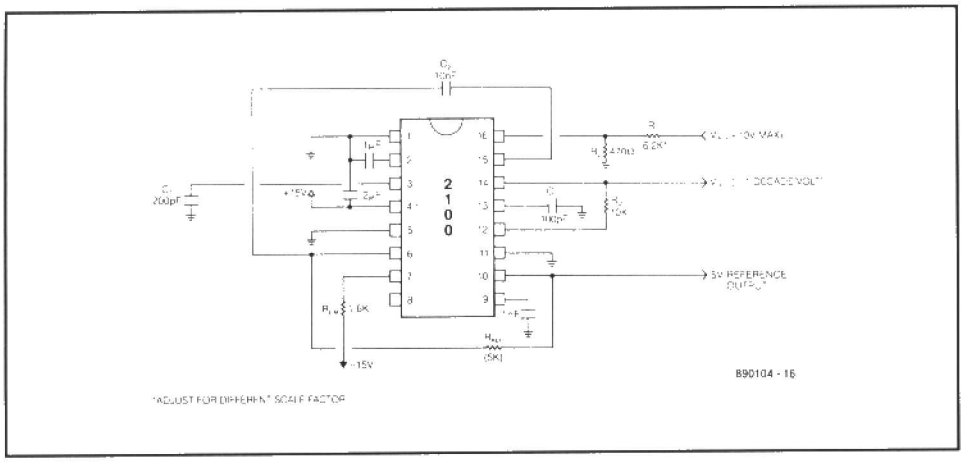
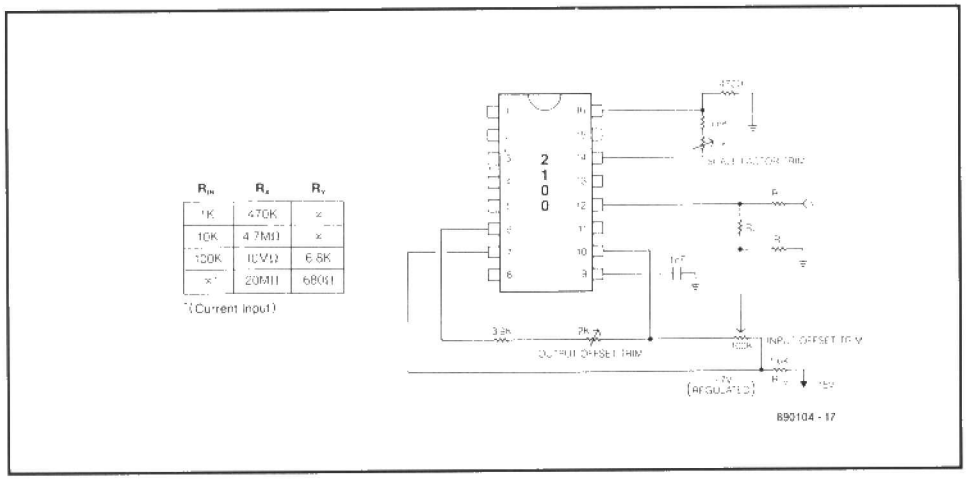


Fig. 5. Antilogarithmic (exponential) amplifier



R_{in}	R_x	R_Y
1K	470K	∞
10K	4.7MΩ	∞
100K	10MΩ	6.8K
∞*	20MΩ	680Ω

*(Current input)

Fig. 6. Trimming the 2100

However, the output amplifier of the 2100 can swing only about 1.5 V below earth and can sink only about 300 µA of current. This causes problems if the reference current is more than 1 decade below the signal current.

If the latter criterion is not exceeded, the circuit of Fig. 3 is recommended. Resistor R3 provides the extra sink current to provide a –1 V output with an additional 10 kΩ load.

If full four-quadrant capability is required, the output buffer shown in Fig. 4 may be added. This will provide a ±5 V output for reference/signal ratios from 10^5 to 10^{-5} (a 10 decade dynamic range).

Antilog (exponential) amplifier

Figure 5 shows the connexions required to generate the exponential function. The input range as shown is zero to 10 V but this can be changed by adjusting R1. The output scale factor is –1 decade/volt but may be changed by adjusting Rout. The bandwidth of the circuit is about 500 kHz.

Trimming the 2100

Figure 6 shows general trimming techniques for input offset, output offset and scale factor. The input offset adjustment may be duplicated for the reference input in the case of log ratio applications.

The input offset trim removes errors caused by amplifier offset and input bias current. The use of the positive and negative reference voltages gives a high rejection to supply voltage changes.

Unlike an opamp, a logarithmic amplifier can not be trimmed with $V_{in} = 0$, because the log of zero theoretically gives an infinite output voltage. A suggested technique is to trim output offset and scale factor first, and then apply a small signal to the input and adjust the input offset trim for correct reading at the output.

EVENTS

IEE Meetings
17–18 Oct — Artificial neural networks (Savoy Place, London)
27–29 Oct — Commercial awareness and business skills for young engineers (London)

Further information on these events from IEE • Savoy Place • LONDON WC2R 0BL • Telephone 01-240 1871

31 Oct – 3 Nov — Aerotech 89 (NEC Birmingham)

Details from the Conference Department • Institution of Mechanical Engineers • 1 Birdcage Walk • LONDON SW1H 9JJ • Telephone 01-222 7899

INPOWER, the Independent Power Generation Exhibition, will be held at the Excelsior Hotel, Heathrow, London. Dates and other details from FMJ International Publications Ltd • Queensway House • 2 Queensway • REDHILL RH1 1QS • Telephone (0737) 768611.

The **TEST + TRANSDUCER** show will be held at the Wembley Exhibition Centre, London, from 24 to 26 October. Details from Trident International Exhibitions Ltd 21 Plymouth Road • TAVISTOCK PL19 8AU • Telephone (0822) 614818.

The **DESIGN ENGINEERING SHOW AND CONFERENCE** will be held at the NEC, Birmingham, from 10 to 13 October. Details from Cahners Exhibitions Ltd • Chatsworth House • 59 London Road TWICKENHAM TW1 3SZ • Telephone 01-891 5051

BLW, British Laboratory Week, will take place at Olympia, London, from 10 to 12 October. Details from Curtis Steadman & Partners Ltd • The Hub • Emson Close • SAFFRON WALDEN CB10 1HL • Telephone (0799) 26699.

The **WORLD MOBILE COMMUNICATIONS IN THE 90S** conference will be held in London on 11 and 12 October at the Hotel Inter Continental. Details from the Financial Times Conference Organization • 126 Jermyn Street • LONDON SW1Y 4UJ • Tel. 01-925 2323.

The **ELECTRONICS DISPLAYS** exhibition will take place at the Wembley Exhibition Centre, London, from 17 to 19 October. Details from Blenheim Online • Blenheim House • Ashill Drive • PINNER HA5 2AE • Telephone 01-868 4466.

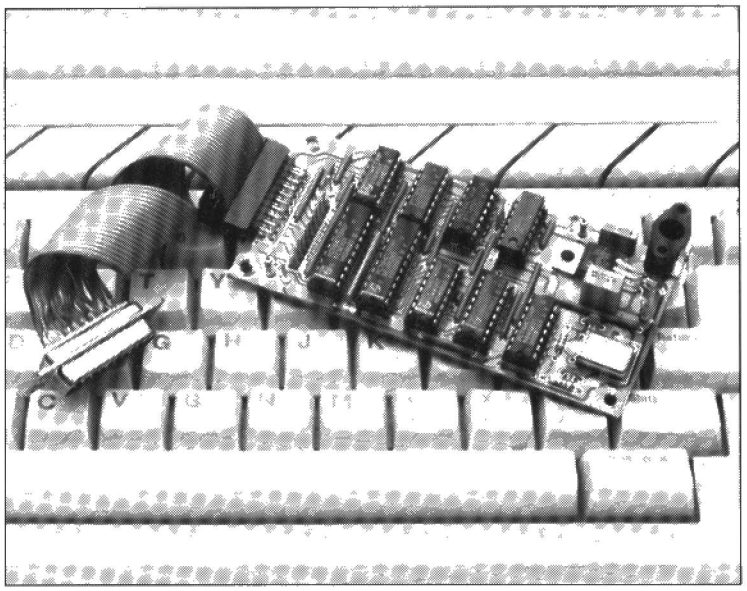
LOGIC ANALYSER WITH ATARI ST

H.J. Schulz

Because of its competitive price, excellent display and the availability of a wide range of software packages, the Atari ST series of home micros has enjoyed a long-standing popularity with a large group of computer users, and has held its own in spite of the influx of IBM PCs and compatibles. The present logic analyser illustrates the capabilities of the Atari ST series for applications other than the most familiar ones, desk-top publishing (DTP) and computer music.

The logic analyser, together with the function generator, multimeter and the oscilloscope, is an essential piece of test gear in an electronics workshop or laboratory. Although a logic analyser is really indispensable for testing and repairing a wide variety of digital circuits, it is often sadly lacking from the home experimenter's test equipment shelf because of its high cost.

The hardware and software described in this article, however, form an affordable test instrument that can provide many of the functions offered by a costly logic analyser.



A computer offers a simpler way to realize a logic analyser than a digital oscilloscope, mainly because the digital (TTL or CMOS) signal levels can be read and processed direct, obviating analogue-to-digital conversion circuits. In most computer-based logic analysers, a number of signals (usually 16, 32 or 64) are simultaneously sampled and displayed on a monitor. Professional logic analysers have a sampling rate of 1 or 2 ns. Lower rates are, however, perfectly adequate for less demanding applications.

Circuit description

The hardware part of the logic analyser is remarkably simple by virtue of the software package available for controlling it. In fact, the main task of the interface circuit shown in Fig. 1 has been reduced to one of signal capturing and timing, so that the sampled levels can be safely applied to the computer, which assumes all other control functions.

The printed-circuit board for the logic analyser has two connectors: K_1, which connects the interface to the DMA (direct memory access) port of the computer, and K_2, which takes the 8 digital signals to be monitored to the relevant inputs of the interface. Two further inputs, CLK and TRIG accept an external clock signal and an external trigger signal respectively.

The DMA bus gives direct access to the computer's memory, allowing high data transfer speeds to be achieved between the computer and external hardware. In most cases, the DMA bus is used for external floppy disk drives, network interfaces, or hard disks. Figure 2 shows the signal assignment, signal direction and pinning of the ST's DMA port. All inputs and outputs are TTL-compatible.

Data exchange via the DMA bus is effected on the basis of certain protocols. The data bits are sent on datalines D0 through D7, which are bidirectional. The logic analyser has an 8-bit register, IC_8, that allows a number of analyser functions to be controlled by the computer, via the DMA bus.

The 4 MHz clock signal generated by quartz-controlled oscillator N_1-N_2 is applied to divider IC_5. Depending on the logic combination applied to the channel selection inputs A-B-C of multiplexer IC_6, output X supplies either 4 MHz, 2 MHz, 1 MHz, 500 kHz, 250 kHz, 125 kHz, 62.5 kHz, 31.25 kHz or the frequency of the signal applied to the external clock input. The maximum frequency of the external clock signal is about 2 MHz.

The signal at the multiplexer output is applied to the B input of monostable multivibrator (MMV) IC_9. As soon as the $\overline{IRQ}$ (interrupt request) line goes low, each clock pulse from the multiplexer is converted to a DRQ (DMA request) pulse for the computer. If this is ready to handle data received via the DMA bus, it responds to the request by actuating the DACK (DMA acknowledge) line. Provided DACK is low, and the DMA bus is set to the read mode, the output of gate N_7 goes low, so that bus buffer IC_7 is enabled via its G input. As a result, data levels available at connector K_2 are passed to connector K_1, and from there to the computer. Each new clock pulse causes the above sequence to be repeated, allowing the computer to read a new 8-bit dataword. The selected clock frequency, therefore, determines the sampling frequency.

8-CHANNEL LOGIC ANALYSER

Hardware:

- 8 TTL channels
- 2 MHz sample frequency
- 31 Kbyte memory
- Selectable sample rate
- External clock input
- External trigger input
- Selectable trigger polarity
- Connects to ST DMA port

Software:

- Data read after triggering
- Selectable trigger polarity
- 6 scroll speeds for data window
- Zoom function
- Pulse timing with cursor counter
- Disk storage/retrieval of samples

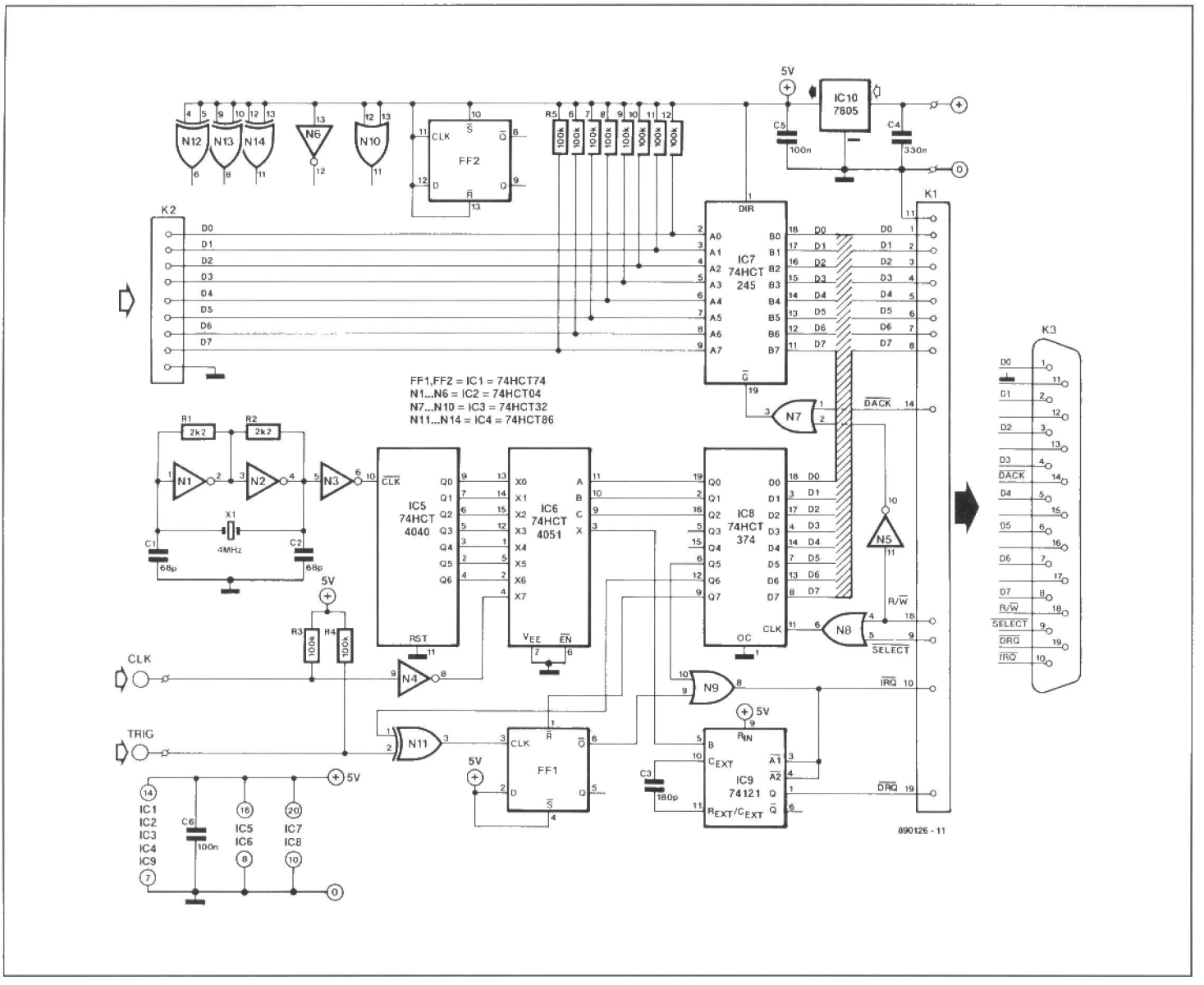


Fig. 1. Circuit diagram of the computer interface, the hardware part of the logic analyser.

Triggering

Correct triggering of a logic analyser is just as important as it is for an oscilloscope. The present logic analyser is triggered by an externally applied pulse. The software allows the trigger polarity (positive or negative pulse edge) to be selected. In the interface, polarity selection is achieved by output Q6 of IC5 controlling one input of XOR gate N11, so that bistable FF1 toggles on positive or negative edges of the trigger pulses. The bistable is set by the positive edge of a trigger pulse, and is reset via output Q7 of IC8.

The external trigger input of the interface is driven by the output signal of a word comparator or any other digital trigger generator. A word comparator supplies a trigger pulse when the logic input pattern matches a preset pattern, and so allows the user to determine which bit combination causes the logic analyser to start reading samples. Subsequently, a buffer is loaded with sampled values. If the buffer is full, the computer halts the analyser, and displays the 8 datalines on the monitor.

Software

The control program developed for the logic analyser is available on floppy disk.

The screen dump of Fig. 3 gives an overview of the available commands and features, which are mostly self-explanatory. The upper part of the screen is reserved for the sampled bit patterns, the lower part for the user interface. Non-used channels have their inputs taken high by a pull-up resistor on the interface board, so that a steady logic high line is obtained.

An entire data window may be stored on to disk with the aid of the SAVE option in the menu. Similarly, LOAD retrieves previously stored windows, which are displayed again for further study.

Options POS and NEG in the TRIGGER block have been discussed already. The TIMEBASE/STEP function allows 1 of 8 sample frequencies to be selected. The sample frequency determines the speed at which datawords are accepted by the computer, and must be set as required by the signals to be monitored.

The MAGNIFIER function is based on software only. The selected magnifier determines the width of the pulses in the data window.

Function SAMPLE enables the trigger input. After actuating it, the first trigger

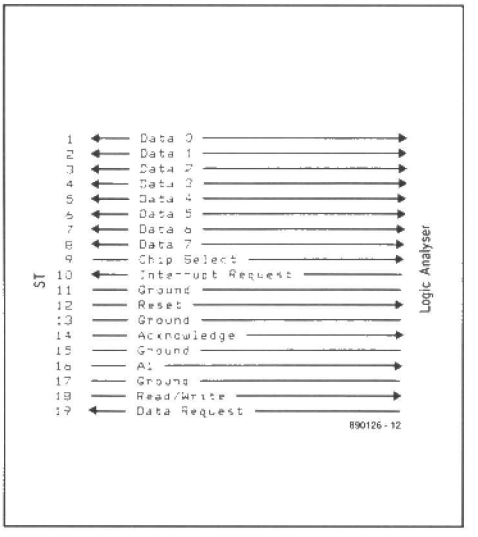


Fig. 2. Signal assignment and pinning of the DMA port connector.

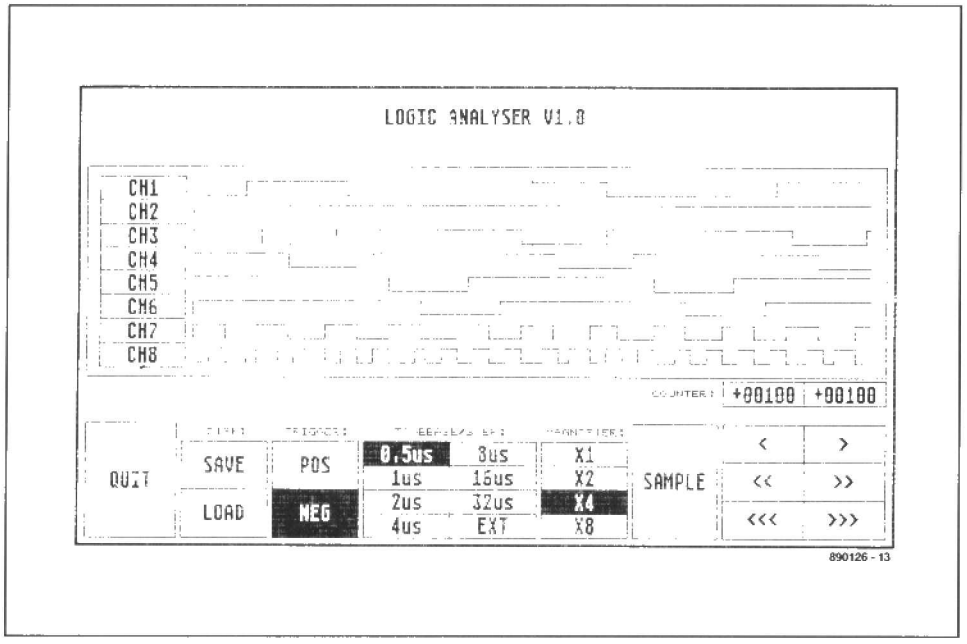


Fig. 3. Screendump illustrating the use of the data window and the available commands. The dotted vertical line in the data window is the cursor.

pulse transition with the selected polarity causes the interface to start reading samples.

The six fields in the right-hand bottom corner of the screen move the cursor in the data window. The cursor position is also indicated numerically in the COUNTER blocks, allowing the time between two events to be measured fairly easily.

Construction

The printed-circuit board for the logic analyser is shown in Fig. 4. Construction is straightforward, and should not present problems since only standard components are used.

Start the construction with the fitting of the wire links on the board. Next, mount all resistors, capacitors and integrated circuits. IC sockets are not strictly required if you trust your soldering skills.

Regulator IC_{10} does not need a heatsink because the current consumption of the interface is relatively low.

Check all components positions and solder joints before connecting the completed interface to the computer.

Construct a 20-way flat ribbon cable for connecting K_1 to the D-19 socket (K_3) on the Atari computer. The pinning of this socket is shown inset in the circuit diagram.

Power the interface from a mains adaptor with 9 V d.c. output.

Test the completed interface by running the associated software. If any faults are found, these must be eliminated before the interface is built into a compact enclosure.

The software for this project is available on a 3½-inch floppy disk under order number ESS 111. Details on cost and ordering are given on the Readers Services page elsewhere in this issue.

FROM ELEKTOR FEBRUARY 1990 P.59 CORRECTIONS

R3,4,5,6,7,8,9,10,11,12 = 100k

C6 = 100N

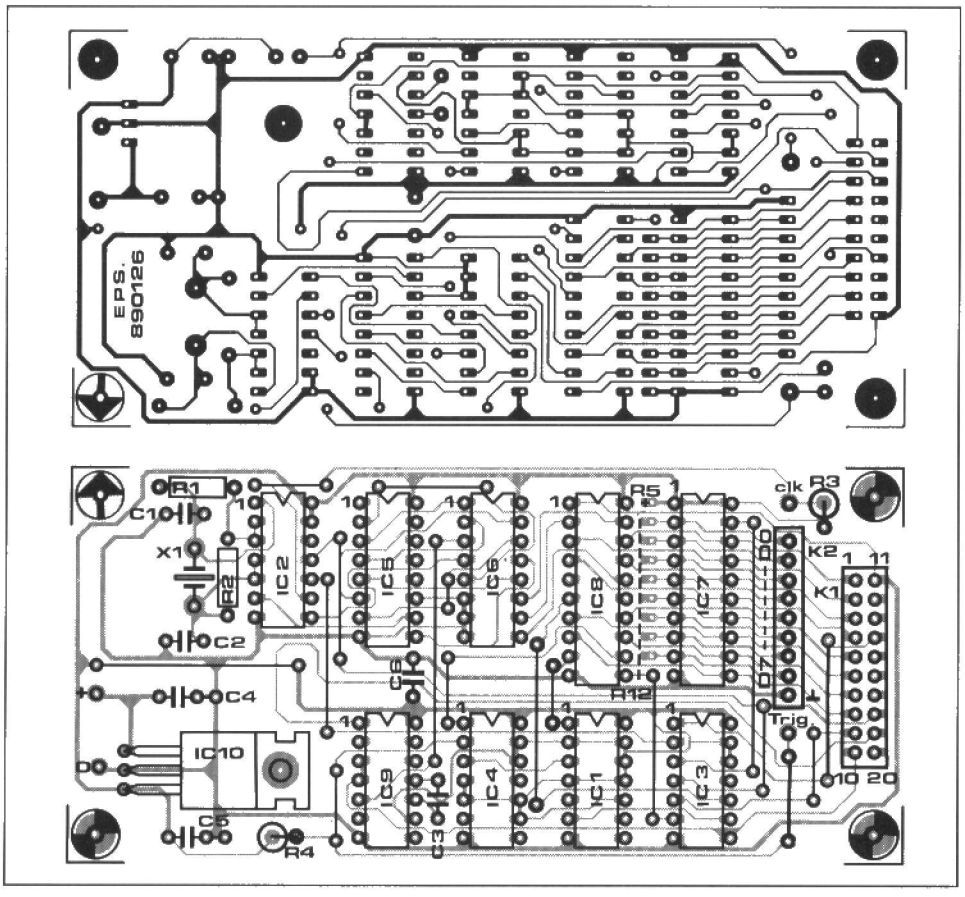


Fig. 4. Track lay-out and component mounting plan of the PCB for the logic analyser.

Parts list

CIRCUIT IS CORRECT

Resistors:
R_1;R_2 = 2k2

Capacitors:
C_1;C_2 = 68p
C_3 = 180p
C_4 = 330n
C_5 = 100n

Semiconductors:
IC_1 = 74HCT74
IC_2 = 74HCT04
IC_3 = 74HCT32
IC_4 = 74HCT86
IC_5 = 74HCT4040
IC_6 = 74HCT4051
IC_7 = 74HCT245
IC_8 = 74HCT374
IC_9 = 74121
IC_{10} = 7805

Miscellaneous:
K_1 = 20-way PCB header.
K_2 = 8-way PCB header.
K_3 = male DB-19 connector (not on PCB).
X_1 = 4 MHz quartz crystal.
PCB Type 890126 (see Readers Services page).
Enclosure: e.g., Heddic Type 222.

PRACTICAL FILTER DESIGN – PART 9

by H. Baggott

Following last month's discussion of Chebishev filters with a ripple of 0.1 dB in the pass band, this month's article deals with Chebishev networks with a 0.5 dB ripple. These have an even steeper cut-off profile than the 0.1 dB types but, as explained last month, the ringing becomes more pronounced.

As in previous articles, five tables are given that contain all the information for the calculation of Chebishev filters with a 0.5 dB ripple in the pass band. As was the case with Table 11, Table 15 can not be used for the computation of an even-order section with equal input and output impedances. For π sections, the table is valid for a ratio of 2:1, whereas for T sections the ratio is 1:2. It all depends on which resistance is used as a reference.

The specific properties of the 0.5 dB Chebishev filter are again shown most clearly by the characteristics in Fig. 47, 48 and 49. The ripple is very evident in Fig. 47, although it should be borne in mind that the left-hand part of the scale has been 'stretched'. Things are therefore not as bad as they may seem: it is only when the ripple exceeds 1 dB that operation becomes troublesome.

The cut-off profile is steep: the attenuation of a fourth-order filter at $2f_k$ is about 33 dB.

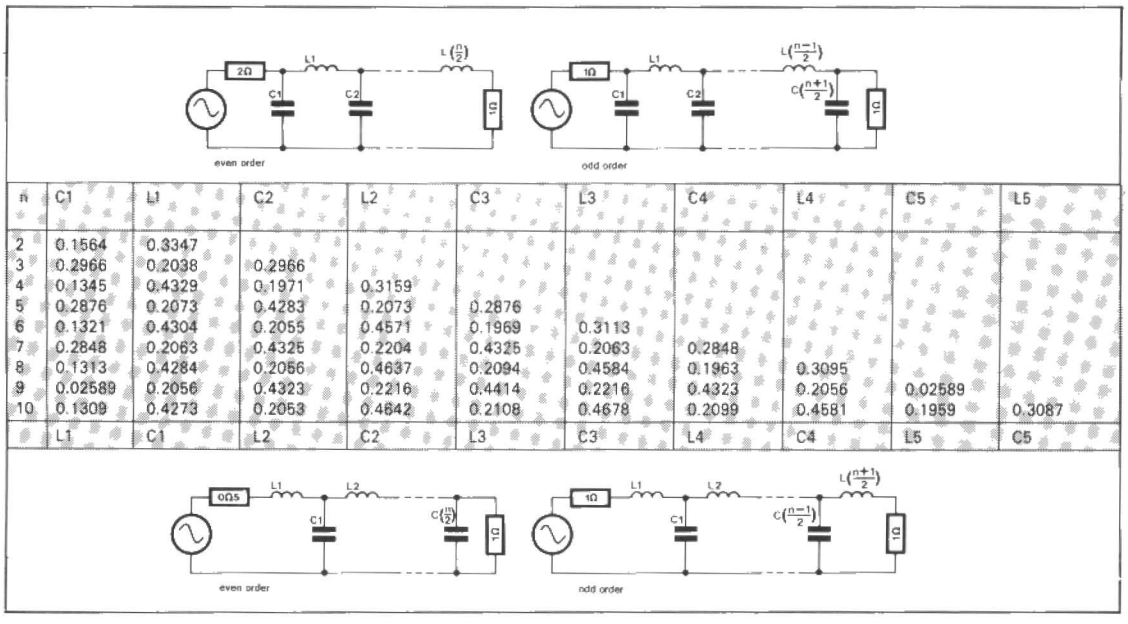
It is interesting to note that the number of 'rings' is the same as the order of the filter.

The delay time characteristic in Fig. 48 shows why the Chebishev filter is not suitable for use in phase linear (audio) applications.

The step response in Fig. 49 shows the ringing, which is comparable to that in

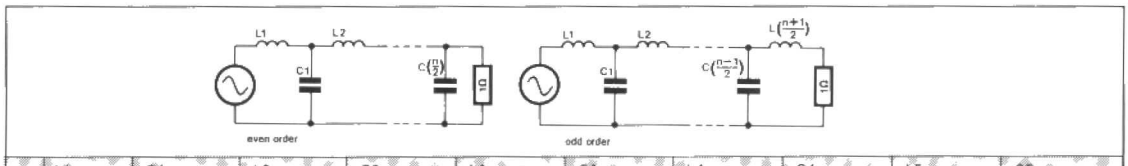
n	real part $-\alpha$	imaginary part $\pm\beta$
2	0.502	0.7278
3	0.2654	0.8913
	0.5309	
4	0.1594	0.9509
	0.3849	0.3939
5	0.1053	0.9788
	0.2756	0.6049
	0.3406	
6	0.07437	0.9941
	0.2032	0.7278
	0.2776	0.2664
7	0.05522	1.0034
	0.1547	0.8047
	0.2236	0.4466
	0.2482	
8	0.04257	1.0094
	0.1212	0.8557
	0.1814	0.5718
	0.214	0.2008
9	0.03379	1.0136
	0.09731	0.8913
	0.1491	0.6616
	0.1829	0.352
	0.1946	
10	0.02747	1.0165
	0.07971	0.917
	0.1242	0.7278
	0.1564	0.4672
	0.1734	0.161

Table 14. Pole locations of Chebishev filters with a 0.5 dB ripple.



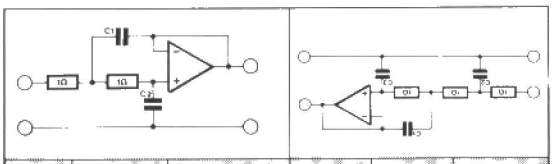
n	C1	L1	C2	L2	C3	L3	C4	L4	C5	L5
2	0.1564	0.3347								
3	0.2966	0.2038	0.2966							
4	0.1345	0.4329	0.1971	0.3159						
5	0.2876	0.2073	0.4283	0.2073	0.2876					
6	0.1321	0.4304	0.2055	0.4571	0.1969	0.3113				
7	0.2848	0.2063	0.4325	0.2204	0.4325	0.2063	0.2848			
8	0.1313	0.4284	0.2056	0.4637	0.2094	0.4584	0.1963	0.3095		
9	0.02589	0.2056	0.4323	0.2216	0.4414	0.2216	0.4323	0.2056	0.02589	
10	0.1309	0.4273	0.2053	0.4642	0.2108	0.4678	0.2099	0.4581	0.1959	0.3087
	L1	C1	L2	C2	L3	C3	L4	C4	L5	C5

Table 15. Standardized component values for passive low-pass filters with an input impedance to output impedance ratio of 2:1 for even-order sections and 1:1 for odd-order sections.



n	L1	C1	L2	C2	L3	C3	L4	C4	L5	C5
2	0.208	0.1551								
3	0.2502	0.2416	0.1483							
4	0.2286	0.3006	0.2421	0.1453						
5	0.2594	0.2769	0.3058	0.2409	0.1438					
6	0.2327	0.3151	0.2833	0.3084	0.24	0.1429				
7	0.262	0.2829	0.3232	0.2848	0.3062	0.2393	0.1424			
8	0.2341	0.3187	0.2904	0.3263	0.2851	0.3059	0.2388	0.1421		
9	0.2631	0.2847	0.3274	0.2926	0.326	0.285	0.3056	0.2384	0.1418	
10	0.2348	0.32	0.2926	0.33	0.2934	0.3262	0.285	0.3053	0.2382	0.1416

Table 16. Standardized component values for passive low-pass sections with negligible source impedance.



n	C1	C2	C1	C2	C3
2	0.3104	0.104			
3			1.7873	0.3581	0.01424
4	0.992	0.02868			
	0.4109	0.2069			
5	0.5059	0.01821			
			1.0889	0.5279	0.04827
6	2.1327	0.01258			
	0.781	0.05957			
	0.5717	0.3057			
7	2.8759	0.0092			
	1.0259	0.03866			
			1.2689	0.7135	0.0748
8	3.7322	0.007017			
	1.311	0.02728			
	0.8757	0.0844			
	0.7425	0.4054			
9	4.7014	0.005531			
	1.6329	0.02036			
	1.0659	0.05442			
			1.522	0.904	0.09963
10	5.7869	0.004472			
	1.9942	0.01584			
	1.2809	0.03829			
	1.0159	0.1078			
	0.9167	0.5053			

Table. 17. Standardized component values for active filters with single feedback path.

Fig. 44.

A worked example

This time we give only one example, but it has two possible solutions.

Design an active band-pass filter with a a –3 dB bandwidth extending from 11.5 kHz to 12.5 kHz. The attenuation at 8 kHz and 18 kHz must be not smaller than 40 dB.

The aim is to keep the circuit as simple as possible. Since no mention was made of the permitted ripple in the pass band, we choose a 0.5 dB Chebishev section, because this has the best cut-off profile.

First, we calculate the centre frequency, f_c:

$$f_c = \sqrt{(f_1 f_h)} = 11{,}990 \text{ Hz}.$$

Next, we must ascertain the complementary frequencies for the –40 dB points to obtain the steepest cut-off combination.

The lower frequency (8 kHz) is complemented by a frequency of:

$$f_2 = 11990^2 / 8000 = 17{,}970 \text{ Hz}.$$

The higher frequency (18 kHz) is complemented by a frequency of:

$$f_1 = 11990^2 / 18000 = 7987 \text{ Hz}.$$

The optimum combination is, therefore, 8000 Hz and 17970 Hz, although the differences are so small that we could use either combination. The –40 dB bandwidth is, therefore, 17970 – 8000 = 9970 Hz.

From the characteristics we must determine how this bandwidth may be achieved with the smallest number of sections.

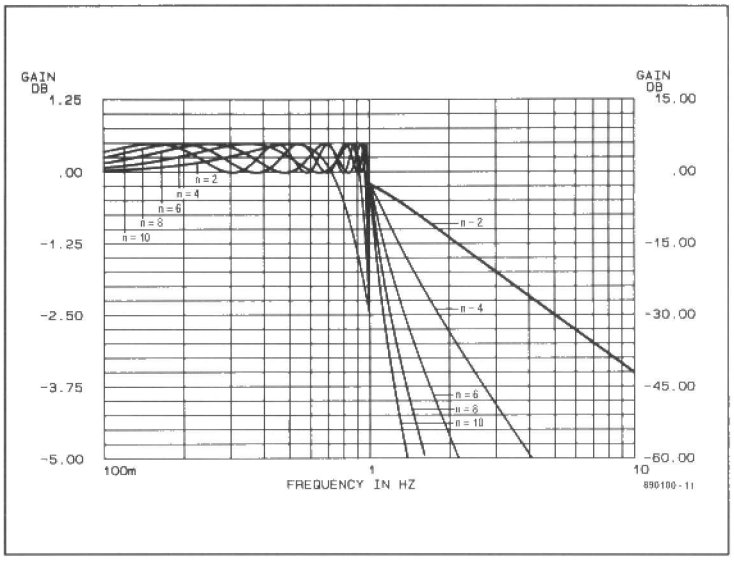


Fig. 47. Gain vs frequency characteristics of Chebishev filters with a 0.5 dB ripple.

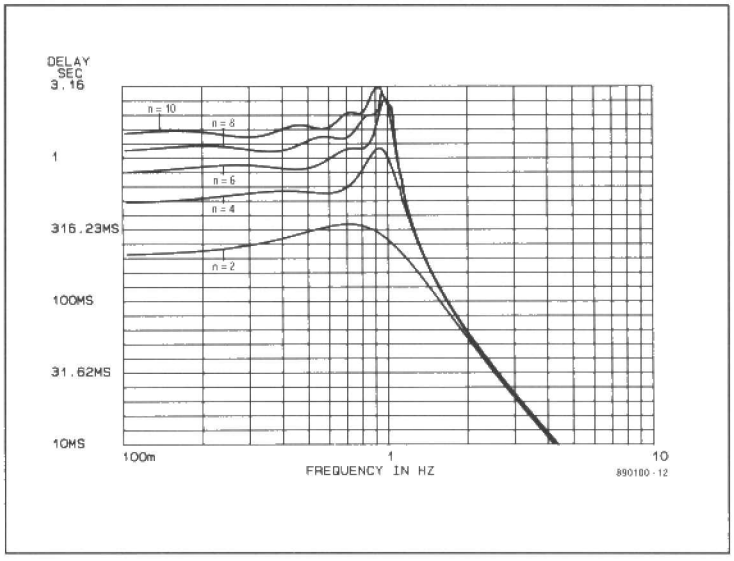


Fig. 48. Delay time vs frequency characteristics of Chebishev filters with a 0.5 dB ripple.

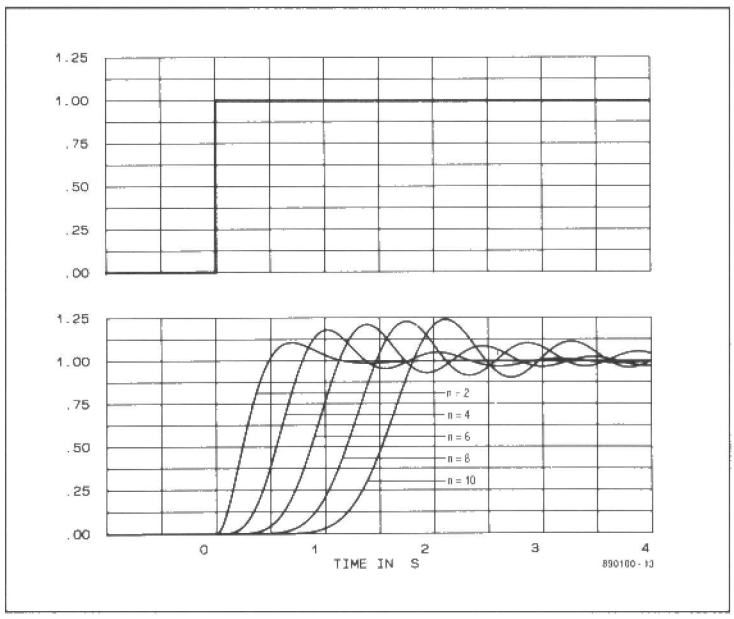


Fig. 49. Step response of Chebishev filters with a 0.5 dB ripple.

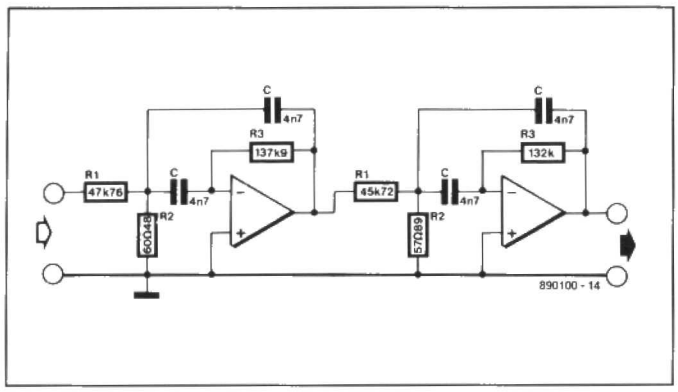


Fig. 50. A second-order active band-pass filter with only one opamp per stage. At higher Qs, as in the worked example, problems soon occur.

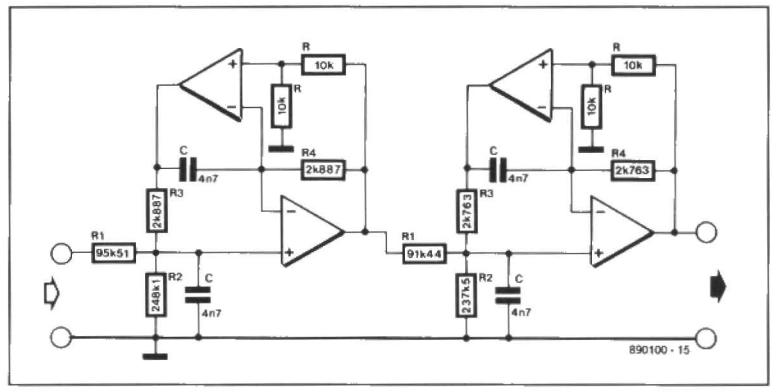


Fig. 51. The same filter as in Fig. 50, but configured as a two-stage double opamp circuit.

For this, we take the ratio of the bandwidth at –40 dB and that at –3 dB:

9970 : 1000 = 9.97.

Using this value in Fig. 47, the attenuation of a second-order filter is seen to be about 42 dB, amply meeting the requirement.

In the first instance, an opamp with multiple feedback paths as in Fig. 30 (Part 5) is chosen. Two of these must be cascaded as in Fig. 50 to obtain a second-order filter.

Before the component values can be calculated, the poles must be ascertained from Table 14:

$-\alpha = 0.502$;

$\pm\beta = 0.7278$.

The Q factor of the filter must be:

$Q = 11990 / 1000 = 11.99$.

The calculations to arrive at the centre frequency, Q value, amplification, and so on, can then be carried out, resulting in:

$C = 0.7817$
$Q_s = 23.89$
$D = 1.022$
$f_{sa} = 11{,}731$ Hz
$f_{sb} = 12{,}254$ Hz
$A_{sa} = 1.444$
$A_{sb} = 1.444$

The component values are then calculated with the aid of the formulas given in Part 5. The value of the capacitor is taken as 4.7 nF.

First stage:
$R_1 = 47.76\ k\Omega$
$R_2 = 60.48\ \Omega$
$R_3 = 137.9\ k\Omega$

Second stage:
$R_1 = 45.72\ k\Omega$
$R_2 = 57.89\ \Omega$
$R_3 = 132\ k\Omega$

In practice, this circuit will function, but the Q of each stage is fairly high. Moreover, the voltage attenuation at the inputs is high enough to cause hum and noise problems unless the highest quality opamps are used.

To obviate these difficulties, a two-stage section based on Fig. 31 (Part 5) as shown in Fig. 51 may be used. This circuit is able to cope with the high Qs.

The calculations to arrive at the centre frequency, Q value, amplification, and so on, remain as for Fig. 50, but the component values will have to be recalculated.

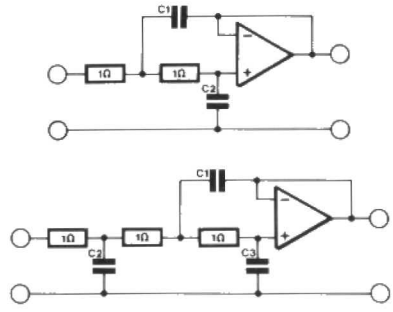
First stage:
$R_1 = 95.51\ k\Omega$
$R_2 = 248.1\ k\Omega$
$R_3 = R_4 = 2.887\ k\Omega$

Second stage:
$R_1 = 91.44\ k\Omega$
$R_2 = 237.5\ k\Omega$
$R_3 = R_4 = 2.763\ k\Omega$

There is no noticeable attenuation at the inputs of this network. It is, however, necessary that the components used are close tolerance types (1%), otherwise the characteristics of the practical filter will not be identical to those of the calculated network.

Correction to Part 8

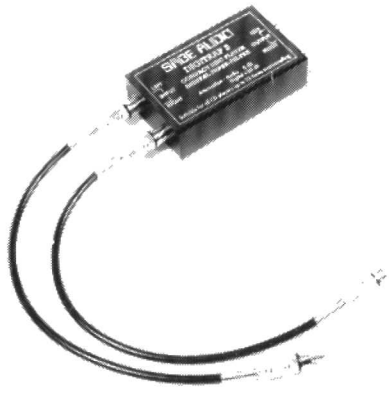
The two circuits shown below were omitted from the top of Table 13 in Part 8. Sorry!



New digital filter from Sage Audio Electronics

'Digitrap' is a new digital filter from Sage Audio that is inserted between the audio output of a CD player and the input of the associated amplifier. It passes the audio signal unattenuated while trapping the digital quantization noise. The consequent lowering of the digital noise floor results in up to 30 dB increase in signal resolution allowing the low-level signal detail te be heard.

It is particularly suited to CD players that use oversampling as these have a greater bandwidth of quantization noise and also less internal filtering. Two types are available: 'Digitrap 1' at £39.95 for CD players with up to 4 times oversampling and 'Digitrap 2' at £59.95 for those with up to 32 times oversampling. Both units are fitted with gold-plated phono input-output sockets and come with low-noise, low-capacitance connecting cables.



Sage Audio Electronics • Construction House • Whitley Street • BINGLEY BD16 4JH • Telephone (0274) 568647.

COMPUTER-CONTROLLED TELETEXT SYSTEM

A. Clapp

The experimental system described allows the loading into a personal computer of Teletext pages, including the ones that are not normally accessible on a domestic TV set equipped with a Teletext decoder.

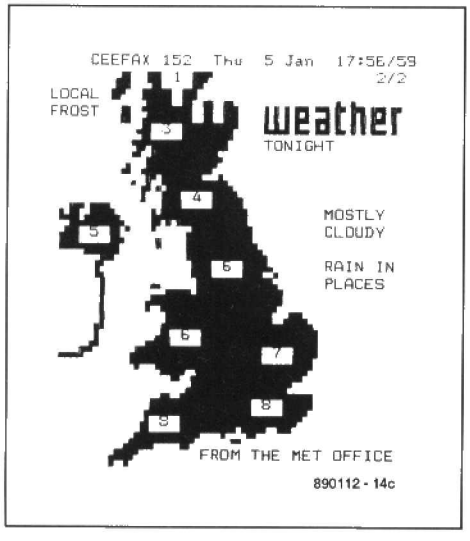
Teletext has been incorporated with television throughout Europe since the mid seventies, with the first published specification jointly issued in September 1976 by the BBC, IBA and BREMA. This initial specification permitted the production of domestic TV sets with Teletext. The specification has continued to develop over the years, and additional facilities have become available.

Teletext 'Level-2' provided multi-language text, and a wider range of display attributes that may be non-spacing. There is a wider range of colours and an extended mosaic pictorial set.

'Level-3' introduced dynamically redefined character sets (DRCS) permitting the display of non-Roman characters, for example Arabic or Chinese. Pictorial graphic characters may also be defined, allowing the composition of improved illustrations for the text compared with earlier levels.

'Level-4' includes full geometric graphics, and requires computing power to generate the display from a sequence of drawing instructions. This permits graphic displays as good as the highest resolution mode of the BBC-B computer. This level offers a colour palette of over 250,000 shades.

'Level-5' is full-definition still pictures, permitting an image of a better quality than achievable from a video camera. It has no losses due to modulating on to a carrier, and no noise added to the picture during transmission.



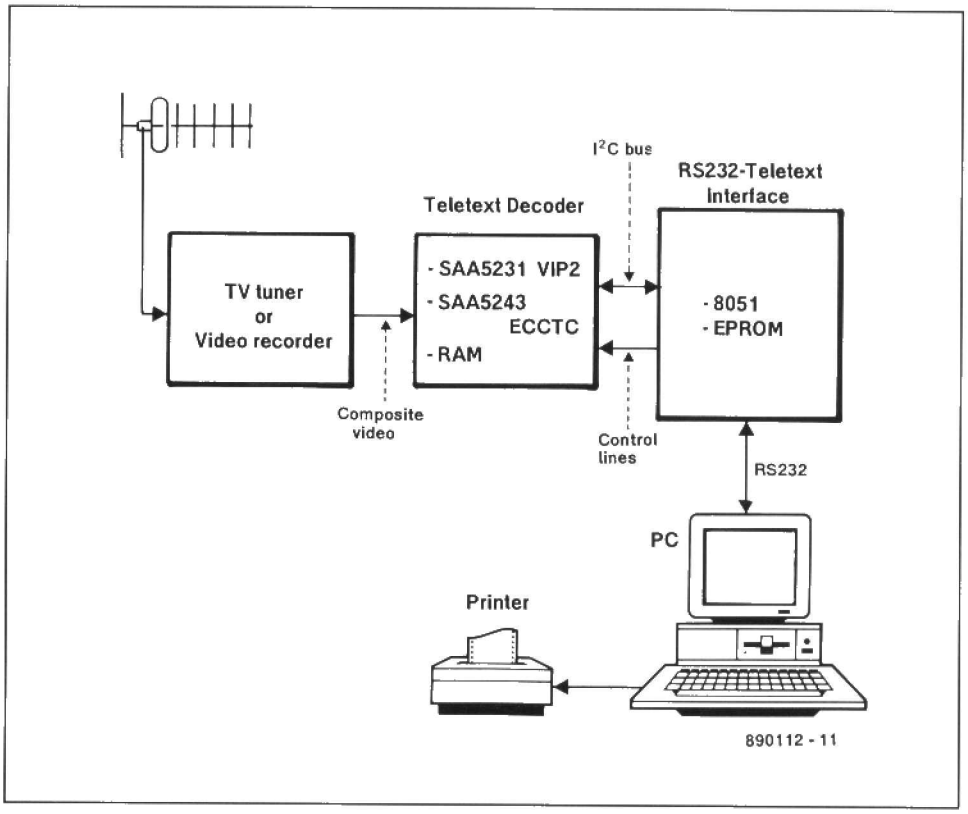


Fig. 1. Block diagram of the experimental system.

Also possible within the system at any level is Telesoftware, which is normally seen as a BASIC listing for BBC computers. It can however be machine code for any computer, and encrypted to limit access.

Levels 4 and 5 exist as specifications, although level 4 was transmitted by the IBA as long ago as 1981. There appear to be no TV sets able to handle these levels, and until the editors of CEEFAX and ORACLE use it, the extra cost would not be worth while. Given the TV producers' liking for computer graphics on everything from weather maps to pop videos, hopefully they will come very soon.

Hidden pages

The specification for Teletext is wider than apparent from the familiar remote control handset. Page numbers, for example, are chosen from a key pad with digits 0 to 9. A displayed page has 24 lines. Less known is the fact that the system can accept key numbers in hexadecimal. This means that page numbers such as 10F could be transmitted and never seen by a home TV set. This permits pages to be transmitted to specially equipped receivers only. The system can transmit 32 rows, 8 of which will not be displayed. Three of these are in fact defined: two are used to simplify and speed up related page selection, and the third carries system information including date, time, channel and, when permitted, a program definition field to enable video recorders to be switched automatically to recording by TV programme rather than time.

The key point is that the specifications and capabilities of Teletext are improving constantly, and an embedded design can not be altered to make use of these developments. In the case of hidden pages and rows, it may be that the originators do not

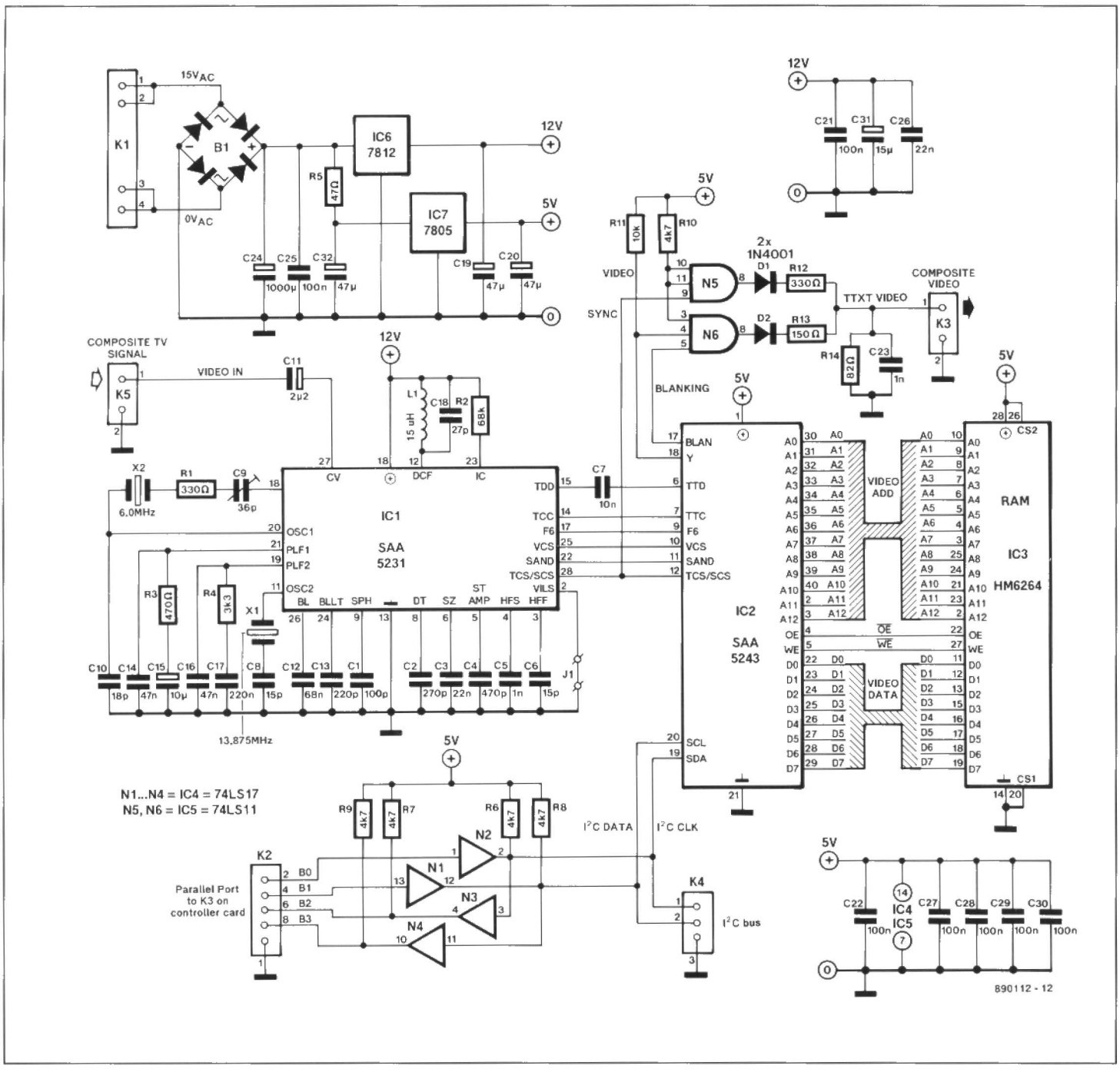


Fig. 2. Circuit diagram of the Teletext decoder card. The monochrome video output is optional, and intended for debugging purposes.

want to make the information generally available.

The Teletext decoder described here can access all definable pages and rows, and make them available to a personal computer (PC) for analysis. The design is split into three units, two of which will be described in detail in this article. These two units are a Teletext decoder and a data and control interface connected to a PC's RS232 port. The third unit in the proposed system is a TV tuner. The block diagram of the system is shown in Fig. 1.

The decoder

Philips Components (formerly Mullard in the UK) have long produced a family of ICs for Teletext, and most TV sets use them. The present decoder is based on two ICs from this family.

The first is the SAA5231 Video Interface Processor (VIP2), an analogue IC that requires quite a few passive components to be attached to make it work (see Fig. 1). The video processor takes a composite video signal from the TV set, and identifies those lines carrying Teletext information. These are subsequently transferred to the digital Teletext decoder IC SAA5243. The data clock is recovered from the Teletext data stream by the VIP2, and passed to the decoder IC. The 6 MHz clock that runs the system is also generated by the VIP2. The 13.875 MHz is divided by two and phase-locked to the Teletext data to become the data clock. Most of the resistors and capacitors around the VIP2 chip are required to extract and phase-control the Teletext data and clock.

The second IC, the SAA5243 ECCTC (Enhanced Computer-Controlled Teletext Chip), is the really clever one. It takes the stream of serial Teletext data, and analyses it. When a new page header arrives, the information is compared with that of the internal registers. If the new header identifies a requested page, it is stored to an area in the attached RAM. The decoder is capable of doing this for 4 unrelated pages, and holding the latest update of 4 Teletext pages at any one time.

The ECCTC also controls the display function of Teletext. Under the control of internal registers, one page in RAM is converted to a displayed page. The video signal is available as RGB TTL levels with separate sync and blanking. A monochrome signal is also available.

The third function of the ECCTC is the one that makes it the choice for this project: the SAA5243 is designed to work on

a computer network, in this case the Philips I²C bus. This is basically a two-wire networking system specifically designed for consumer electronics. Each I²C bus compatible IC has a unique address built in, and a set of communication protocols to use. The IC monitors the network, and recognises when it is being talked to. In response to certain commands it interacts with the sending device on the bus.

In the present circuit there are only two devices on the I²C bus: the decoder and the microprocessor. A connector is provided on the decoder board to make the connection to other I²C devices possible if experimentation is desired.

The operation of the ECCTC chip and the I²C bus is relatively complex. By contrast, the hardware required to implement the decoder chip in an I²C environment is remarkably simple. The I²C bus has strict protocols, and the timings must be adhered to. The ECCTC has several registers that have to be loaded correctly before anything will happen. At power-up there is little evidence of life from the device, and the display will not even have sync, let alone a default page of Teletext.

It is common for complex devices to be controlled via a piece of software called a *device driver*. With such a driver, the user has available a set of high-level commands that allow all the functions to be performed without the need of detailed knowledge of that particular function. A full discussion of the operation of the ECCTC and the I²C bus is so detailed as to exceed the scope of this article. Software is available to drive the decoder card, and extract from the transmission any byte, row or page of Teletext. Readers wishing to know how this is done in detail are referred to the Application Notes mentioned at the end of this article.

The third essential IC is a 4-to-2 line converter that connects the Teletext decoder the I²C network. The 4 lines go to the external processor that transmits data and clock up and down one pair, and receives data and clock back from the decoder.

A composite video output is available on the decoder board to display monochrome Teletext direct from the decoder. The video output is useful for debugging the system because switching between grabbed pages is instantaneous while transfer via the bus takes about 8 seconds. The few additional low-cost components needed to implement the video output seem worthwhile even if the facility is rarely used. They can be omitted, however, from the circuit without affecting the rest of the operation.

The composite video is taken from a Rediffusion tuner unit that can be used to drive the decoder card direct. The video output from a VCR should also prove all right. The decoder has a link that alters the input level required to drive the card. In the event of the source not supplying enough signal, a buffer may be required to connect the video source to the decoder card. Use of a tuner unit based on a SAW (*surface acoustic wave*) filter is well worth considering. Teletext is particularly sensitive to phase distortions, and SAW filters are a considerable improvement over *L-C* IF circuits.

The ECCTC chip has 8 channels, of which 4 are capable of grabbing a page of Teletext as it is received. The operator selects the channel to be current from 0 to 3. The required page for the current channel is selected, and that channel will continuously grab the updates for that page, even when the current channel is changed. The only exception occurs during page transfers to the host computer. The status line, row 25, must be examined to determine when the required page has been received. When a new page is requested, the old one is cleared, including the status line. This is then examined repeatedly until the new page received is signalled. The new page is then transferred in ASCII to the host computer, which has to do the graphics code conversion.

The use of the other 4 ECCTC channels is detailed below.

Downloading Teletext pages on a PC

The function of the controller card is to respond to instructions received on the RS232 link to a PC, and to return Teletext information to a host computer. All the timing and protocol requirements needed to transfer information on the I²C bus are handled by an 8051-based controller card (Fig. 3).

Commands from the host computer are in the form of a single letter defining the requirement, followed by a qualifying number. Available commands are listed in Table 1. Page selection, for example, is made by the host PC sending the letter P followed by a 3-figure page number. The controller card then transmits the command to the Teletext decoder card. The controller repeatedly examines the status line in the decoder until the requested page is received. The page is subsequently transferred from decoder memory, via the RS232 interface, to the PC, which allows the page to be stored on disk, or to be printed.

R*hhh*	examine row in hex
A*hh*	examine row in text
C*h*	channel select
P*hhh*	page select
D	display page
H	print page
F	file on disk
T	timed page
ESC	exit program

Table 1. Commands for the IBM PC control program.

The commands allow the full capabilities of the decoder to be available to the host PC, while keeping traffic on the RS232 interface to a minimum. To allow a wide variety of computers to be used, the bit rate has been set fairly low at 1200/s. This means that a page of Teletext takes about eight seconds to transfer. Pages are repeated roughly every 20 seconds on Teletext, so a selected page takes about 30 seconds to receive from request.

Channel selection allows 1 of the 8 channels to be selected as currently attached to the interface. The current channel is also the one used to form the on-card

Col.	0	1	2	3	4	5	6	7	8	9
B0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
B1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
B2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
B3	PU3	PT3	C4	MT3	HU3	C6	C10	C14	0	0
B4	ERR	ERR	ERR	ERR	ERR	ERR	ERR	ERR	/FND	0
B5	0	0	0	0	0	0	0	0	0	S
B6	0	0	0	0	0	0	0	0	0	0
B7	0	0	0	0	0	0	0	0	0	0

PU	units
PT	tens
MAG	magazine
MU	minute units
MT	minute tens
HU	hours units
HT	hours tens
C4–C14	transmitted control bits
S	page is being looked for
/FND	page has been found
ERR	transmission error in byte

Table 2. Row 25: status line format codes.

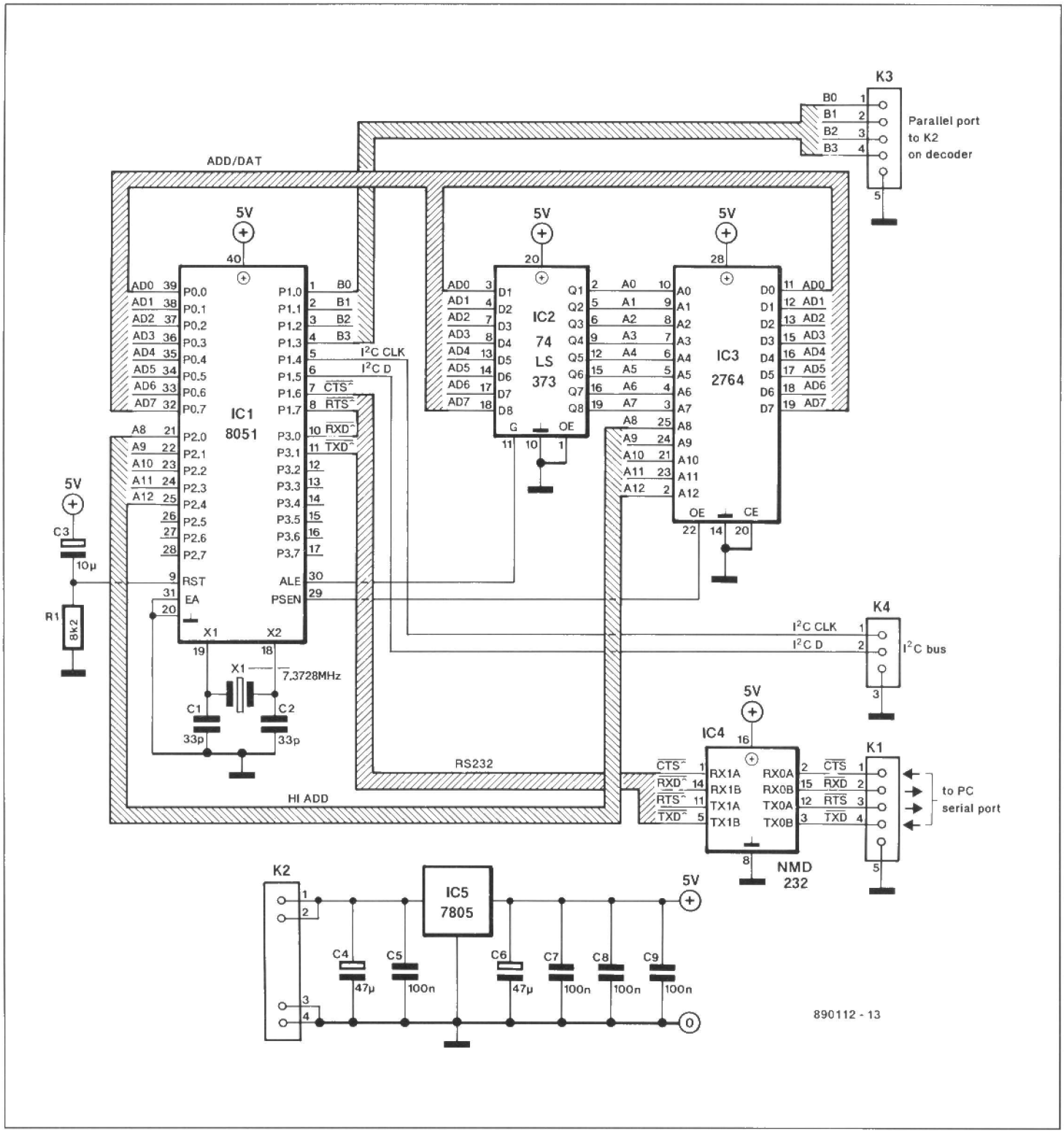


Fig. 3. Circuit diagram of the PC interface card that holds the 8051 controller, EPROM with firmware, and the RS232 level convertor chip.

monochrome display, if used. As already discussed, ECCTC channels 0 through 3 are Teletext pages of the form seen on the TV screen. Channels 4 through 7 are extensions of the first 4 pages. Commands such as D (display) and H (hard copy; print) use the currently selected channel as the source of data. Page selection can only be achieved for channels 0 through 3.

The controller transfers pages as blocks of 24 rows of 40 characters. The embedded commands of Teletext are removed, and the 7-bit code is extended to 8 bits to allow for direct representation of graphics.

The choice of graphic characters to use may pose a problem in that there is no standard for Teletext graphics. The author used an Okidata-80 as well as an Epson MX-80F/T printer. Both of these have a character set that includes all Teletext shapes. Unfortunately, the codes are different for each printer. The IBM clone used was fitted with a Hercules type monochrome display adapter. This has very few graphic characters, so only an approximation of Teletext shapes is possible. To allow the use of two printers, the control card has the option of two translations of the Teletext page. Each will result in a print-out that is an accurate black-and-white copy on the appropriate printer. The display has only 6 graphic characters that are similar enough to use. Since there are 64 Teletext graphics characters, the host computer translates the graphics character into 1 of the 6 which is most appropriate. The resultant displayed page is in fact better than one would expect. Since the quality of this display is a function of the host computer configuration, users should be able to write their own graphics translation routines to maximize the fidelity of the representation. The commands that transfer

text do so with all colour information removed. If the computer is capable of colour, the hex transfer command must be used to ensure that the decoder supplies unaltered data for translation into a format suitable for the display used. An accurate monochrome display is always available from the decoder card. Pages saved to disk are in the printer format, and can be printed out at any time for an exact copy.

Users who have other printers will need to make modifications to permit a true copy. Provided the printer is capable of producing the Teletext graphics set, one of the approaches will work. If the graphics of the printer are ROM-based, the character codes supplied by the RS232 interface card must be translated into appropriate printer codes. This will be a one-to-one translation carried out with the aid of a look-up table which a number of PC communications programs, such as Procomm, have available. If the printer is a type with a RAM-based character set, such as the Epson FX-80 or compatible, the best approach is to reprogram it to emulate an Epson MX-80F/T.

Since the purpose of the present decoder is to permit examination of the data without pre-conceptions, and allow non-ASCII data to be read, two other transfer modes are available.

The first of these allows transfers of a specified row in ASCII with graphics modified as with the full-page mode. The other transfers a specified row in hexadecimal format as it appears in memory, allowing the host PC to process a page of unmodified data.

These two options can be demonstrated quickly by examining channel 4: three lines will contain data; one has plain ASCII text, one Hamming-modified numbers relating to the ASCII text, and the third contains plain hexadecimal data containing status infirmation on the transmission, including time, date and channel.

PC interface card

The RS232 interface and controller card shown in Fig. 3 is based on the 8051 microcontroller from Intel. The 128 bytes of internal RAM are sufficient to hold all information for control and temporarily program data. An external EPROM addressed by a latch Type 74LS373 holds the machine code that forms the control program. The UART (universal asynchronous receiver/transmitter) in the 8051 coupled to Newport Components' single 5 V RS232 interface chip Type NM232CD result in a simple, yet reliable, RS232 link. The NM232CD has an on-board ±15 V converter.

Practical use of the system

Having built the decoder and the interface, you are in a position to get more out of Teletext than from a standard television-based system. The ability to save

Fig. 4. Some more sample print-outs of Teletext pages downloaded with the proposed system.

pages to disk and edit them creates the ability to build up a database. All weather charts, for instance, over a certain period could be collected if meteorology is a hobby.

The BBC transmits computer programs via Teletext, and these are available with the present system. Once pages can be transferred to disk, it becomes possible to save an entire magazine. One on disk, access to pages is much faster than waiting for the page to come up in the transmission. This is particularly true if a sub-page is requested. A sub-page can be specified by selecting the required page, and setting the time-page option to the sub-page number, i.e., timed page 0003 for sub-page 3 to display this only.

For a first challenge of beating the hiders of information, users may like to consider the Televox page, currently on page 777 of ITV on HTV and presumably elsewhere. This is an interactive page where a subscriber can control the display of information via voice control on the telephone. On first entry to the service, the user is given a timed page number to set his Teletext to. Then information is sent as a timed page transmission, immediately followed by a blank screen on a non-timed page. The effect is that if the timed page is not set, the pages appear for only a fraction of a second and can not, therefore, be read. The odds of guessing the correct page are small, and as subscribers log on and off it changes.

For further reading:

1. *Broadcast Teletext Specification*, September 1986. BBC, IBA, BREMA.
2. *Level-4 Enhanced UK Teletext*. R.H. Vivian, IBA UK.
3. *Enhanced Computer-Controlled Teletext Circuit SAA5243*. Philips Components Technical Publication 255.
4. *World System Teletext Specification*.

The software developed by the author may be ordered through the Readers' Services under order number ESS113. A 5¼-inch 360 KByte MS-DOS formatted floppy disk is supplied, containing:

- the control program for IBM PCs and compatibles equipped with an RS232 port;
- the contents of EPROM IC_3 on the RS232 interface card. The code is provided in the form of a file in Intel-hex format.

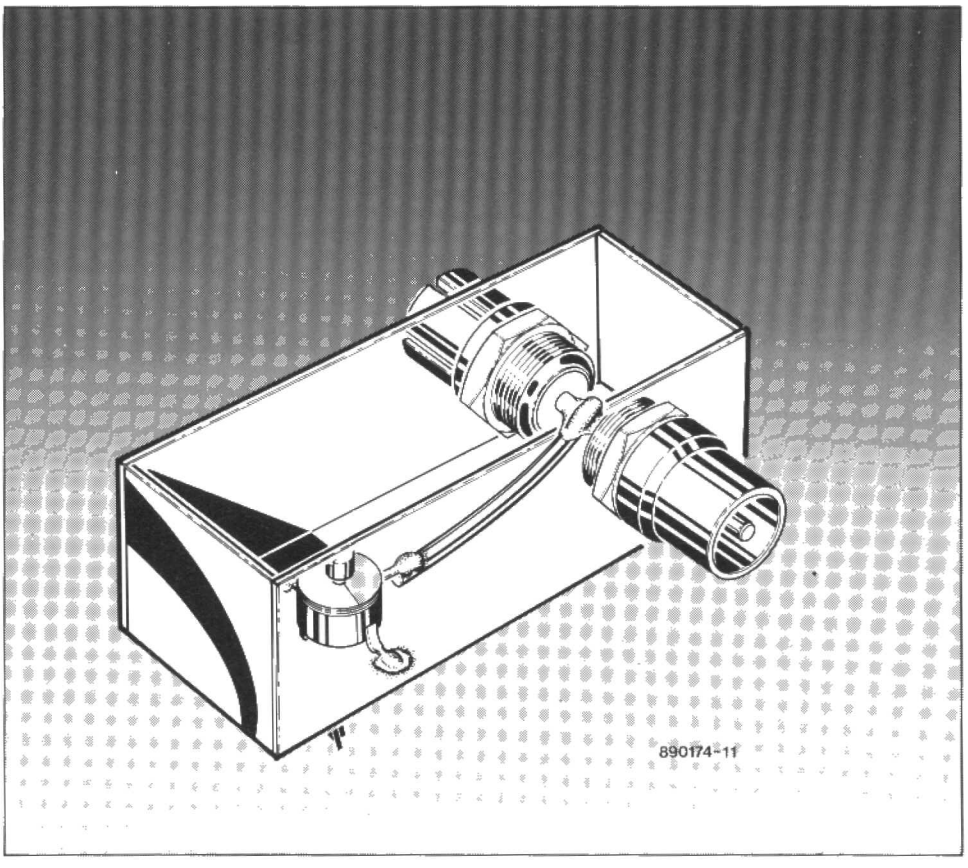
Details on ordering the package are given on the Readers' Services page elsewhere in this issue. We regret that no PCB artwork has been designed for the present project.

Note: the SAA5231, SAA5243 and the 13.875 MHz quartz crystal used for building this project should be available as spare parts from authorized Philips Components Service Centres.

UHF CHANNEL TRAP

J. Bareford

Powerful repeaters for cellular radio and paging systems, or a strong local UHF TV transmitter, can wreak havoc with the reception of your favourite TV channel. This is usually caused by excessive field strength and resultant intermodulation in the aerial booster or the UHF input stages of the TV set. Cancel the interference once and for all with this simple two-component notch that covers the entire UHF TV band.



Ghost pictures, moiré effects, poor synchronization, colour corruption, picture inversion and even complete receiver detuning are but a few of the awkward problems suffered by TV owners having their own roof-mounted aerial installation, but unfortunate enough to live close to a transmitter site with UHF stations on it.

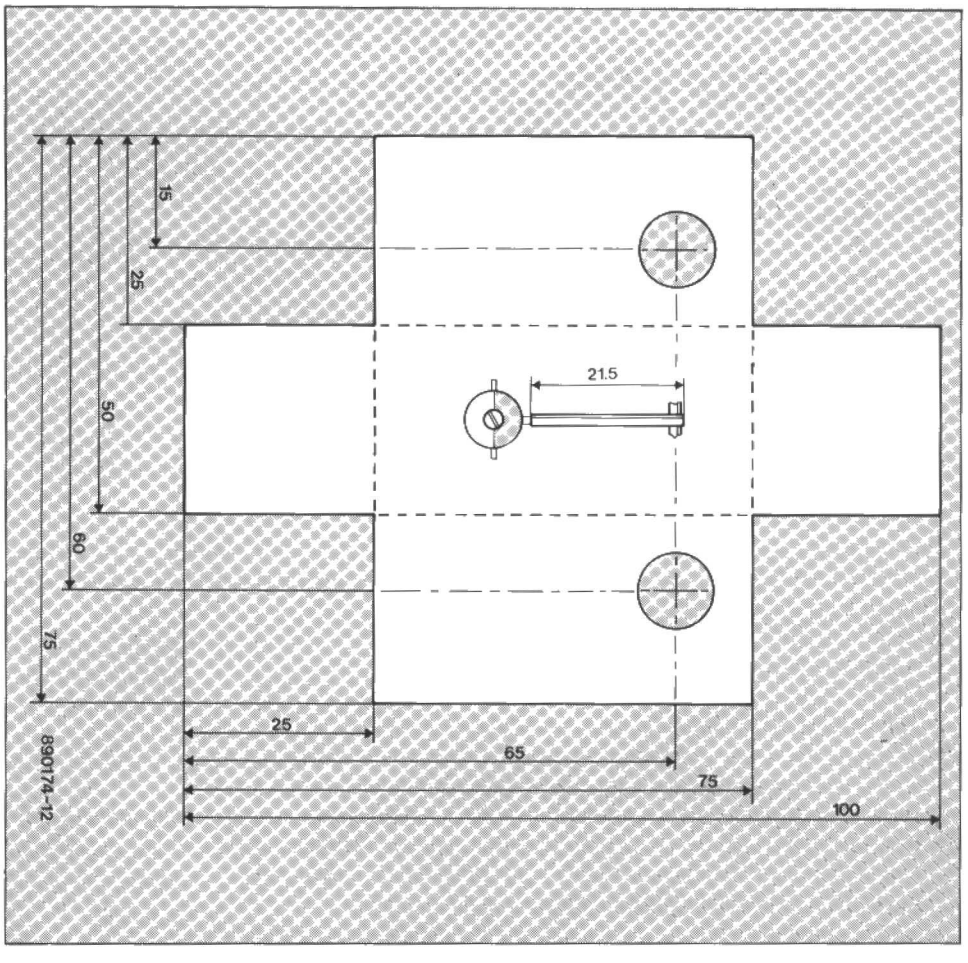
Problems may arise almost overnight when you find that a particular TV channel suddenly has a lot of interference on it, or is simply replaced by an moving pattern with accompanying buzz on the sound channel. On investigating the matter, it may be found that a UHF cellular radio repeater has been installed recently on a nearby elevated building. The strong signal in the 600 or 900 MHz band blocks the preamplifier in your aerial booster or TV set, or, more precisely: the d.c. setting of the preamplifier is shifted to the extent that the stage acts as a mixer or even a demodulator or frequency multiplier (varactor effect).

Similar problems may occur if a strong TV signal blocks reception of a relatively weak programme on a nearby channel.

30 decibel down

Receiver overloading may be prevented by suppressing the strong, unwanted component in the input frequency spectrum. The present circuit does this with the aid of a series *L*-*C* filter that can be tuned to the interfering frequency. The filter acts as a high-Q notch, offering a suppression of more than 30 dB at the resonance frequency.

As shown in the drawing of Fig. 1, the inductor is a length of 1 mm dia. silver-



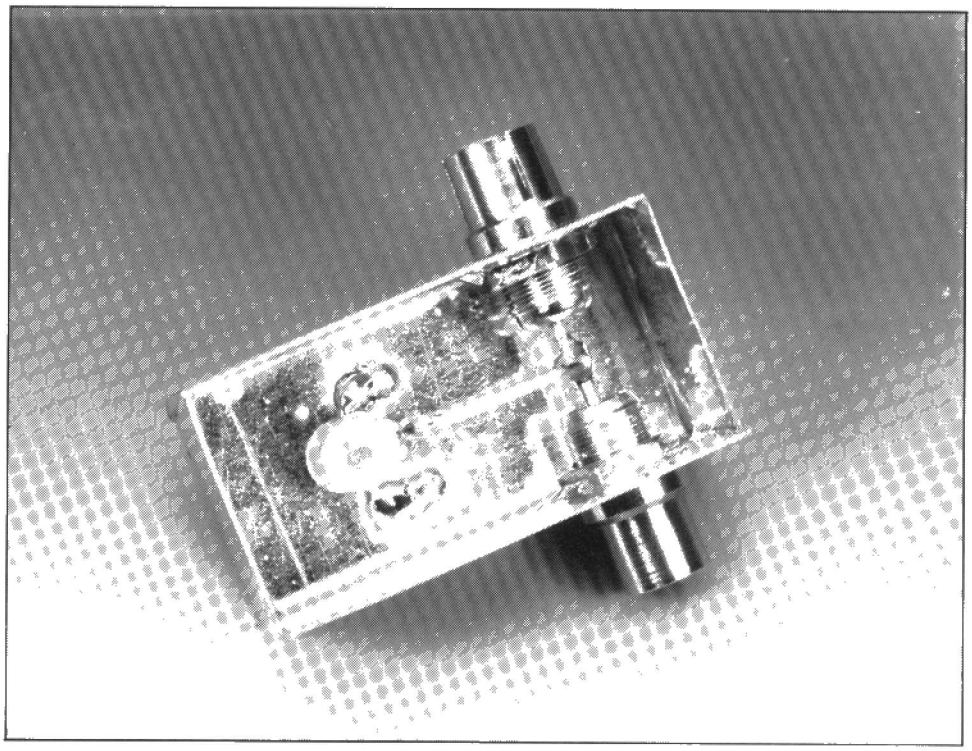
plated wire connected to a 5.5 pF PTFE foil trimmer (colour code grey, Philips Components). The stator terminal of the trimmer is bent forward and soldered to the inductor, while two rotor terminals are soldered direct to ground. This *L-C* combination covers most of the UHF TV frequency range (approx. 470–870 MHz), and gives far better results than, for instance, a quarter-wavelength coax stub.

The trap is housed in a screened enclosure made from sheet metal (tin-plate or brass). Coax sockets enable the trap to be installed in the cable leading to the input of the aerial booster. Do not fit the trap between the output of the booster and the input of the TV set — it has no effect there because the interference is caused in the booster!

One socket on the trap may be replaced by a coax plug to enable the unit to be plugged direct on to the output of the coupling/filter unit, if used.

Alignment is simple: tune to the TV channel you want to watch, and adjust the trimmer until the picture is free from interference. The adjustment is fairly critical due to the high Q factor of the *L-C* filter. If there is more than one source of interference, each of these must be suppressed with its own trap, tuned to the relevant frequency.

Alternatively, if you want to block out a particular TV channel permanently whose reception is otherwise all right (cable networks), adjust the trap for maximum suppression. The TV channel will vanish into noise as you reach the channel frequency. Remember that each channel to be suppressed needs its own trap, unless one acts on a number of channels simultaneously, which is not likely to occur on a cable TV system.



ELECTRONICS SCENE

Extended coverage for BBC TV Europe

BBC TV Europe is a simultaneous relay of the BBC-1 service broadcast in Britain, with BBC-2 programming replacing feature films and purchased material, to give the European viewer an 18-hour per day service of the best of the BBC at the same time it is seen in the UK.

Satellite transmissions of BBC TV Europe began in June 1987, following an agreement between the Danish Telephone Companies and the BBC. The service was extended to Norway later in 1987 and to Sweden in 1988. As of April 1st of this year, BBC TV Europe is transmitted from an east-spot transponder of the Intelsat-VF11 at 27.5 degrees West.

From its start in 1987, BBC TV Europe has steadily attracted more viewers, and now reaches over a quarter of a million households via the Scandinavian cable networks. The use of the east-spot transponder, however, allows direct-to-home reception also if a dish of 1.2 m or larger is used.

BBC TV Europe, like the BBC in the UK, does not carry advertising. Therefore the signal is scrambled and the cost recovered by making a charge to cable companies or direct to home viewers. The SAVE decoder required is available through local agents from Sat-Tel.

BBC Enterprises Limited • Woodlands • 80 Wood Lane • LONDON W12 0TT. Telephone: (01 743 5588). Fax: (01 749) 0538.

Intel unveils industry's first EISA chip set

Intel's 82350 EISA bus chip set consists of two system board devices that provide 100% compatibility with the EISA bus. In addition, Intel is supplying a bus master device for add-in cards, and a bus buffer device that integrates system board glue logic. Included in the new chip set are the 82357 Integrated System Peripheral (ISP) and the 82358 EISA bus controller (EBC),which recognizes and works with both the 32-bit 386 and i486 processors.

Intel also plans to provide the 83252 EBB for those manufacturers seeking higher integration for the system board. The EBB contains buffering logic for any one of three modes, including address, data and parity control, replacing as many as 17 TTL components. Though not strictly required for EISA compatibility, the EBB will help system designers meet critical EISA timing demands.

Intel Corporation (UK) Ltd • SWINDON. Telephone: (0793) 696000.

Eutelsat participates in Olympus communications experiments

Eutelsat, the European Telecommunications Satellite Organization, and operator of four Eutelsat-1 telecomms satellites, is an active participant in the definition, application and assessment of the communications experiments to be conducted on the recently launched Olympus experimental communications satellite.

Eutelsat has proposed 22 experiments to the European Space Agency (ESA) to be conducted on Olympus. A total of 17 are for the 20/30 GHz payload, four for the 12/14 GHz specialised payload and one for the DBS payload. These experiments will include teleseminars, news gathering, data distribution to microterminals, SS-TDMA and narrowcasting. The first experiments are expected to start in mid-October.

Eutelsat • Vanessa O'Connor • Tour Montparnasse 33, avenue du Maine • 75755 Paris Cedex 15 • FRANCE. Telephone: +33 (1) 45384747. Fax: +33 (1) 45383700.

SCIENCE & TECHNOLOGY

Advanced implant system for VLSI fabrication

by Bill Pressdee, BSc, CEng, MIEE

In the last two decades, integrated circuit technology has invaded most areas of business, consumer products and manufacturing. Its growth has indeed been phenomenal and almost exponential with the element density: nearly quadrupling every two years. This has been the result of several revolutions in the development of semiconductor devices. These have moved on from transistor-transistor logic (TTL), to emitter-coupled logic (ECL), to negative metal-oxide semiconductors (NMOS), and in the last few years to complementary metal-oxide semiconductors (CMOS), in which very large scale integrated (VLSI) chips of one-quarter or one-half million elements are not uncommon.

A similar story can be told of the growth of memory devices up to the most recent bi-polar types, including dynamic random access memories (DRAMS) of up to 16 Mbit capacity and above. As the circuit density has grown more compact, the semiconductor manufacturing techniques have become increasingly sophisticated to meet the requirements of precision in fabrication and reliability in operation.

The fabrication of a VLSI chip, measuring a few tens of millimetres on a silicon substrate is a complicated affair. The VLSI is a complex three-dimensional device, the strata of which are built up by a series of processes involving several chemical substances and a series of photolithographic masks that define the patterns to be transferred to the wafer as photoresist.

Fabrication process

A pattern is fixed, generally by ultraviolet radiation, the unfixed portion being subsequently etched away to allow deposition on the substrate. Precise alignment of the mask appropriate to each stage of the fabrication is paramount, as is the cleanliness of process operations. Careful attention must be paid to the temperatures of deposition and annealing to minimize the out-diffusion of impurities from their layers.

The predeposition diffusion process is one in which a product lot of wafers – loaded into a slotted quartz wafer carrier and introduced into an open-end high temperature furnace tube – is subjected to a flow of dopant transported along the tube by a carrier gas. This is often nitrogen mixed with oxygen, which permits the impurity to reach the wafer surface as an oxide.

This process has now largely been replaced by ion implantation. By accelerating a beam of ionized impurity atoms in a vacuum to strike the wafer surface, the ion implantation technique enables a precise quantity of impurities to be introduced into the substrate. The impurities may be inserted selectively in areas where there is an absence of surface masking material. They can be prevented locally from reaching the substrate by photoresist or a thermal oxide layer of sufficient density.

An ion implanter needs to generate a high current level of the required ion type to reduce processing time. The ions may be produced by any method that endows the atoms with sufficient energy to surmount the ionization threshold, generally by collision between high energy free electrons and atoms of the gas. A radio frequency plasma can be created by an electron field between a hot filament cathode and an anode, and confined by a permanent magnet.

The passage of the atoms through the plasma enables the ions so produced to be accelerated into a beam. This beam is shaped and introduced into the target chamber where it performs a raster scan of the mounted wafer. The beam power and ion dose must be carefully controlled to correspond to the depth of implant required.

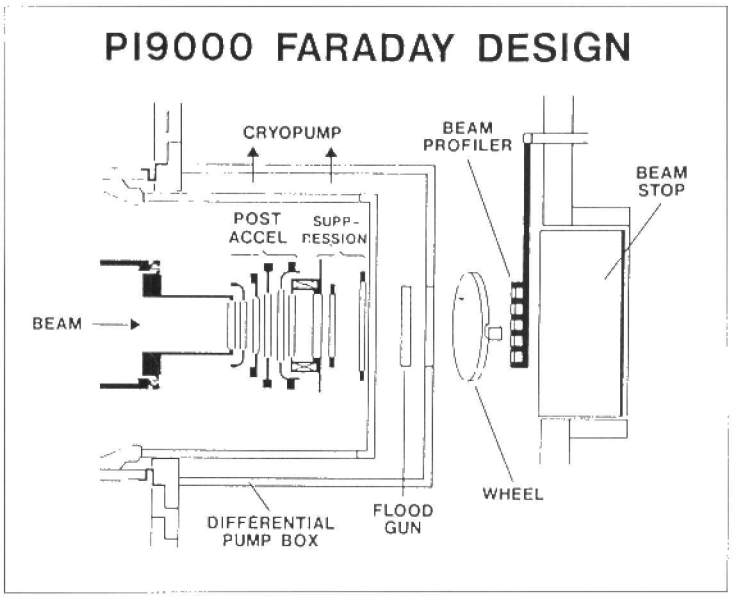


Diagram of the Faraday region of the PI-9000 implanter

Greater flexibility

The precision implanter (PI)-9000 was introduced in September 1985 and brought a new dimension to ion implanters in the context of precision, reliability and throughput. The design of the machine took account of the progress of VLSI towards CMOS devices and also chips containing both CMOS and bi-polar devices.

The fabrication of an advanced CMOS device may require as many as 11 implants, four of which would be at high dosage. On the other hand, the VLSI design may require shallow junctions with boron implants of 10 keV, although such thin gate oxides are a potential source of damage caused by charging effects.

These and other considerations pointed to the need in the PI-9000 for flexibility to accommodate rapid changes in dose, energy and implant species. With beam currents of up to 30 mA and a voltage range of 10 to 180 keV, the machine can handle virtually any implant requirement.

At the time of the PI-9000's introduction, the implanters of even modest current capabilities were subjecting wafers to high power and high charge densities, causing damage to photoresist and oxide layers. However, even with three times as high a beam current as other implanters, the 9000 generates less than one-third the pulse power and charge density, while the photoresist integrity is ensured over its full power specification and beyond. The scanning system spreads the power over a large area and incorporates very high scan speeds. The ultimate wafer temperature is

further reduced by a water-cooled planar heat sink.

The system uses a Freeman source with an extraction voltage of up to 50 kV, decelerating to 20 kV for analysis, and a multi-gap post accelerator that is very tolerant of high pressure transients. Accurate dose control is provided by monitoring the DC current falling on the beam stop when the wheel is out of the beam.

Control of the scanning system is independent of beam current, making dose and dose measurement exempt from the effects of neutralization, secondary electrons associated with wafers, and electrons from the electron flood gun, which is turned off during beam monitoring. The Faraday region also includes a beam profiler for measuring beam shape and position that can be used prior to each implant.

Fewer breakages

The PI-9000 was the first implanter to introduce planar wafer holding, in which the centrifugal force of the spinning wheel holds the wafers in contact with the heat sinks. Its other advantages include:

- better cooling;
- greater uniformity;
- reduced contamination and wafer breakage
- the ability to implant over the whole wafer area.

During photoresist implants, the chamber pressure rises owing to the out-gassing of hydrogen from the photoresist material. One of two cryopumps fitted is used to pump the post-accelerator region, making it very stable electrically even at high out-gassing rates. By careful design of the temperature control system, the wafer temperatures are kept at below 40 °C.

The system processes wafers up to 150 mm in batches of 25, loaded on to the vertical processing wheel. Automatic loading is via a cassette-to-cassette handling system that allows up to five cassettes containing 25 wafers to be placed in the vacuum load lock. Clean room access to the PI-9000 is limited to the load lock chamber and the light-pen-operated video control screen.

Other measures to ensure a clean wafer environment include: sputtering traps; dedicated resolving apertures to reduce cross-contamination; and wafer paddles to remove major sources of contamination and particles. The system maintenance requirements are low; hardware and software are modular in design; full diagnostics, maintenance prompts and self-calibration routines are provided.

Superior wafer handling

The new PI-9200, introduced just over a year ago, is substantially the same as the PI-9000, but has several new hardware and software features and an upgraded performance as a result of three years of operational experience with the earlier machine. The new model includes features incorporated as upgrade kits for the 9000 to improve system reliability, made possible by careful failure monitoring and analysis.

The handling system has been redesigned to take wafers up to 200 mm, the wheel batch size has been reduced to 17, although throughput exceeds that for 150 mm wafers on the 9000. The implanter has a higher performance source and the load lock chamber has been redesigned to reduce gas flow turbulence and particulates, as have the gas vent and pump-down ports.

Internal parts that analysis has shown to be particulate-generating have been eliminated and the particulate level has been further reduced by a new cleaning routine for the load lock and the wheel chambers.

A new control computer has been introduced and the software response times have been improved considerably, while the data collection capacity has been enhanced. The new Autobeam software enables the process engineer to specify any number of recipes to meet the needs of special devices. Each is identified by a simple code number. All the engineer has to do is to specify the number and load the cassette; the Autobeam then takes control of the fabrication.

The Precision Implanter is designed and produced by Applied Materials • Implant Division • Foundry Lane • HORSHAM RH13 5PY • England • Telephone (0403) 53316.

ELECTRONICS SCENE

More Automation for Electronics Manufacturing

Reduced manufacturing times and costs are in prospect for electronics companies as a result of a new computer integrated manufacturing (CIM) software package from Racal-Redac.

Nowadays, most electronics designers use computer-aided engineering (CAE) and computer-aided design (CAD) systems to engineer and lay out their printed-circuit boards (PCBs). The output of such systems, a finished PCB layout, is usually provided via a pen plotter or photoplotter in the form of hard-copy artwork.

However, there are two major areas of inefficiency in using hard-copy artwork to set up a PCB manufacturing process. Firstly, the generation and necessary photographic duplication of the artwork is costly and time consuming. Secondly, the PCB design produced on the CAD system may not meet the constraints on board shape and complexity imposed by the manufacturing process. This will lead to costly reworking of the original design, and possibly to a great deal of wasted effort in trying to set up a manufacturing process for an impossible design.

Racal-Redac's 'Visula CAM (computer-aided manufacturing)' consists of a series of programs that allow PCB designs to be taken directly from its Visula Plus CAE/CAD system (or from non-Redac systems via the standard Gerber transfer format), optimized for the manufacturing process and used to automatically program today's high-technology manufacturing tools such as auto-assembly machines and automatic test equipment.

The most innovative aspect of Visula CAM is its variety of post-processing interfaces. These interfaces allow a PCB design to be post-processed into a data format that can be used to drive the tools used in PCB manufacturing directly.

Electroplating PCBs with Copper

A high-speed acid-copper process that offers excellent deposit distribution for PCBs has been introduced by PMD Chemicals. 'Procirc 971' offers a current density of 20–80 A/ft^2 (1.8–7.4 A/m^2) to make it possible to plate board types selectively that previously could be plated only at relatively low current densities.

The process is suitable for closely packed surface-mount boards; boards that have large areas of ground plane together with isolated tracks; and boards that have a large variation in plating area from side to side. It will plate down holes with a 6:1 depth-to-diameter ratio and give an even coating on surfaces and holes.

'Procirc 970' is a similar solution specifically intended for multilayer boards. It offers the same quality of deposit but improves the depth-to-diameter ratio to 20:1 while still giving nearly even deposit thickness ratios. Its operating current density is 5–25 A/ft^2 (54–270 A/m^2).

OPEN SYSTEMS

by Pete Chown

The growth in standards for computing must be one of the most significant developments of the last few years. The term 'Open Systems' has come to refer not just to the original idea of being able to interconnect different makes of computer, but also to a whole range of products mainly centred on Unix and X-Windows. Sun Microsystems' NFS is often included, although this is really a proprietary system that has become generally accepted.

At the heart of all the OSI applications lies the standard itself, which is what allows them to interchange information, typically over a thin-wire Ethernet. The standard was one of the first systems to be based on a layered model.

The layered model

A layered model is really a form of structured programming, in that high-level operations are separated from low-level operations. Rather than being simply top-down, however, it is split into a vertical stack, so that the higher levels are cut off from the lower levels at certain points.

An accurate interface is defined between all of them, so that a message is passed down at the transmitting side and up at the receiving side.

The layers used in the OSI standard, with the operations they perform, are:

7 – Application. This provides the front end of the system. It controls the actual sending of information down the lower layers and obtains the message from the application program that asked for it to be sent.

6 – Presentation. This layer puts the data provided into the standard format to be sent. It handles data encryption.

5 – Session. It is the job of this layer to ensure that both devices know when communication starts or comes to an end. It must therefore tell the receiving computer that a session (this may be logging on or it may just be sending a message) is starting and also when it has finished. This is particularly important if there is likely to be a significant delay between blocks of data. In that case, it can not be left to time out, because the delay would be very long. This sitution may be encountered if a message is being sent over the packet switch network, where delays can be encountered.

4 – Transport. The purpose of this layer is to decide what the most cost-effective way to send a message is. It does not have any control over the route that the message takes through the network. It will apply such other considerations as urgency and the availability of resources.

3 – Internet. This layer decides on the best route through the selected network for the message to take. The layer could well be on a computer different from that which originated the message: suppose a message is sent on to the packet switch network by the transport layer. It is the responsibility of a different computer to control the route through the network, because individual customers have no control over that.

2 – Dataline. This handles retransmission of corrupted communications and checks CRCs or parity bits (which allow the receiving computer to check the integrity of the data).

1 – Physical. This is the actual device driver that transmits the data on to the hardware interface between the computers.

In many applications, the layers are not distinct: for example, someone may produce a single chip that handles error checking and interfacing, thus joining the dataline and physical layers. In addition, some companies, notably IBM and DEC, have their own version of the standard that predates it: the standard was designed to pull together the various proprietary standards emerging. The layers in these may have different names as shown in the table below for Decnet.

You would be excused for asking what possible advantage there could be in this complex setup. The answer is that it is now possible to conceive of, say, two session layers intercommunicating directly, because the layers below form an interface in their own right. As you go down to lower and lower levels, this interface simply moves nearer to the hardware. Each layer in itself is fairly simple, so that writing an interface based around OSI is not the formidable task it would be without it being split up into a vertical stack.

Layered models also state what is implicit in every interface, even if these are not designed around such a model, in that it needs to be possible for higher level functions to assume that lower level functions have been carried out – that CRCs have been checked, for instance. Before a CRC can be checked, it must, of course be determined that the message is legitimate electrically, so that for an RS232 interface, for example, a byte is framed by start and stop bits correctly. It is thus seen that a layered model follows on from what is really common sense.

Name Designed by	OSI CCITT/ISO	Decnet DEC
	Application	User network application
	Presentation	User network application
	Session	Session
	Transport	End-to-end transport
	Internet	Routeing network
	Dataline	Ethernet
	Physical	Version 2

The application of OSI

The major growth area in computing in the last few years has been in the market for workstations. These are cost-effective ways of computing since they avoid the need of large concentrations of computing power, which are expensive. They depend, however, for their effectiveness on good communications. On a conventional system, communications are provided fairly easily because everyone is working on the same machine. Consequently, the workstations have standards that probably are more emphasized than in any other area of computing.

For this reason, OSI has become associated with workstations and the thin-wire Ethernets they often use for data communications. It is in this sector of the computer market that some of the most imaginative uses have been found for the new protocols.

The graphics standard

The purpose of the graphics standard is to relieve large computers of the work involved in producing graphics to present the results of the programs they are running. It also relieves communications links of the load of transmitting thousands of individual pixels. Instead, certain instructions are sent to local workstations over a thin-wire Ethernet, and these workstations then control the production of the actual image. This technique is referred to as remote procedure calling, because graphics procedures can be called by a remote machine. The code trans-

mitted may the same whatever the receiving machine.

Once the image has been received by the workstation, another advantage becomes apparent. Some of the things that workstations are very good at are desk top publishing and graphics applications, so the pictures obtained from the remote machine can quickly and easily be incorporated into documents being prepared locally (this also relieves large machines of word processing, which, owing to the overhead in switching between tasks, they are very bad at).

Anyone who has used Aldus Pagemaker or MacDraw will be aware of the way in which shapes can be moved around on the screen, as distinct from a 'painting' program where a shape is merely stored as a collection of pixels on the screen. This is another advantage of the graphics standard, because the graphics sent to you by a remote machine can be manipulated locally: you might decide, for instance, that you wanted your pie-chart twice as large. On a conventional system, this would result in large pixels becoming visible where small ones had doubled in size. With the new system, however, all the co-ordinates and sizes can be doubled, giving rise to an accurate chart at four times the area.

Network filing system

The network filing system was devised by Sun Microsystems while everyone else was trying to reach a consensus. This move, brilliant commercially, but bad for effective standards, gave Sun the lead when it became accepted at least as a de facto standard.

This system allows you to work on one machine and use files distributed around a thin-wire network. What you do is to set up a logical directory on your machine that actually corresponds to a directory on a remote machine. The fact that the directory is not local is invisible to the user once that link has been set up.

A similar, but less powerful, system is used by Microsoft for MS-NET. This predates the Sun system by quite a long time, but there are several problems: firstly, the machine providing the files has to be tied up as a dedicated file-server; secondly, the remote directories are mapped on to local drives – each remote directory is thus placed at the level of being a different physical device. This limits the number of remote directories to 26, which is probably not too much of a problem, but it makes the system inelegant and confusing.

Distributed document architecture

The DDA has been set up to allow a document to contain several different files in such a way that the merging of these files is invisible to someone looking at the document. These files could, of course, be on a remote machine if the system were used in conjunction with NFS. At present, it is available only on DEC machines running DEC-windows (a version of X-windows with extensions. The extensions are there to make it difficult for users to change to other X-windows systems. This technique has been used by all the major workstation manufacturers).

This technique opens up a whole range of possibilities. For instance, it makes it possible to design documents that update themselves automatically when something changes, say, a graph. A new run of simulation could, therefore, cause the report relating to it to update automatically as well (it can not, however, rewrite the conclusions drawn from the graph!).

The technique is more efficient in terms of storage than conventional documents. Suppose you have a large illustration that has been 'pasted' into a document prepared on a DTP system. This illustration is then stored in the document file and also in its original form to allow it to be changed if necessary. With a distributed document system, the illustration is stored only once, and the document derives its illustration from the same file.

This system also has some disadvantages: it is, for instance, not possible to have one file that contains a document. This makes it more difficult to e-mail it to someone. Then there is a danger of interconnected webs of files growing up, which are hard to manage because it is much more difficult to say whether a file is finished with. Furthermore, it is possible for a file to belong to more than one document.

These drawbacks become more serious if the constituent files are not even on your machine: suppose you have a file that is offered to somebody remotely and this third party incorporates it into a document without taking a copy of it. You might then conclude that the file is finished with and erase it. This problem is more likely to occur if people working on the same project are routinely given access to your files. It makes it much more important for strict control to be exercised over which files can be assumed to be left there and which not.

Documentation standard

Go into any large organization and you will discover the endless problems of moving documents between different word processors. There is, consequently, a proposal between several large computer companies to set up a standard for transferring documents. This standard, however, is still at the proposal stage.

The idea is that there be a uniform way of storing the margin settings, page lengths, inserting headings, and so on. It seems unlikely to catch on, however, because it relates to text-only documents, and not to DTP output files or documents with graphics inserted into them. It seems improbable that anyone will want to accept a system that can not cope with these types of document.

There are two ways of implementing the documentation standard. One is to use a native-mode editor that works directly on files in this format. The other is to use a conversion program written for a particular word processor that converts files to that format, and then another conversion program to convert the files back to the format required for the destination word processor.

Unix and X-windows

Unix and X-windows are not really OSI-based applications, but are very important for the success of OSI. They form a standard operating system, based on C, that allows programs written for one workstation to run on another. This is very important, because it permits the workstations to become program development tools: the code is then run on a more suitable destination machine. Also, in the volatile workstation market, it is impossible to be really confident about where any of the smaller operators will be in a few years' time. It helps manufacturers to sell their products if users know that they can change to another manufacturer fairly easily. This is, of course, not the attitude taken by IBM who have traditionally blocked standards (even ASCII!) because these allow people to buy non-IBM machines. It is, of course, true that what makes sense for smaller manufacturers does not for larger ones like IBM and DEC who try to get their own standards adopted. Increasingly, however, even these large companies are being forced by user pressure to support OSI.

Bringing it all together

We have looked at OSI and a wide variety of workstation and network-based applications. The large flood of applications depends entirely on OSI and Unix, which makes it clear how revolutionary the combination of these two has been.

I will now consider one example of the use of this combination that brings together many of the things discussed in this article.

The example is a financial report of a company that will contain a general text written by the general manager or managing director, graphics produced by the production manager or director outlining the efficiency of a production process and text and graphics produced by the accounts department showing the overall financial situation of the company. Assuming that it is important for the document to be kept up to date, a distributed system is used.

The general manager, or his assistant, would produce his text, which contains references to the files for the graphics and any additional text. It would not be essential, and in practice it would almost certainly not be the case, to use the same word processor that the other texts are prepared on, as long as the documentation standard is used.

All the parts of the document would update themselves automatically, so long as they did not change so radically as to make the author's conclusions meaningless. One problem with large-scale distribution as encountered here would be the large load on the thin-wire Ethernet.

Let us now consider what would happen to a copy of one of the graphs as it moves through the layered model. Firstly, the message would be passed to the application layer (the message will already be in graphics standard form) on the sending computer, which would fetch the message from memory and send it on.

The presentation layer would encrypt the data if necessary: it would probably not do any protocol conversion because the message is already in a standard form.

The session layer would then (via the lower layers) tell the session layer on the receiving computer that a message is starting (notice how the session layers can be regarded as intercommunicating directly). It would then send the message to the transport layer and tell the receiving computer that the message had been sent. Note that what could be an entire session is only used for one message in this case.

The transport layer would have little to do in this example since only one method of transport is available: the thin-wire Ethernet.

The internet layer would then decide on the most efficient and cost-effective route through the networks if there were more than one connected via a bridge.

Finally, the dataline layer would add CRCs and other checking information and the physical layer would send the message.

On the way to the receiving computer, all the layers would perform the operation in reverse. The first item sent would be the session start information and this would be passed on until it came to the session layer that would note that a message was starting. The rest of the message would then be passed on, and finally the session end information would tell the session layer to end the message.

NEW BOOKS

Electronics IV - Second Edition
by D.C. Green
ISBN 0 582 02183 9
275 pages – 246 × 189 mm
Price £9.95

The second edition of this successful book provides an up-to-date text of modern analogue electronics for HNC or HND students in Electrical Engineering, Telecommunication Engineering, Electronic Engineering or to those studying for the City & Guilds Telecom (271) Higher Course. The corresponding digital electronic requirements can be found in *Digital Electronic Technology* (2nd edition) by the same author.

It will also prove of great benefit to anyone else requiring a comprehensive introduction to modern analogue electronics.

Longman Scientific & Technical • Longman House • Burnt Mill • HARLOW CM20 2JE.

Digital logic gates and flip-flops
by Ian R. Sinclair
ISBN 1 870775 06 6
192 pages – 215 × 135 mm
Price £8.95

This book is intended for students, technicians and any one else seeking a firm foundation in digital electronics. It is not a book for the constructor, but rather for those who want to design and troubleshoot digital circuitry with considerably more understanding of principles than most constructors. Therefore, topics such as Boolean algebra and Karnaugh mapping are explained, demonstrated and used extensively.

No background other than a basic knowledge of electronics is assumed: the more theoretical topics and many working examples are explained from the beginning.

The book concludes with an explanation of microprocessor techniques as applied to digital logic.

PC Publishing • 4 Brook Street • TONBRIDGE TN9 2PJ.

The IEE wiring regulations explained and illustrated
by Brian Scaddan, IEng, MIElecIE
ISBN 0 434 91823 7
96 pages – 210 × 147 mm
Price £ 7.95

This book should be read in conjunction with the 15th Edition of the *Regulations for Electrical Installations* issued by the Institution of Electrical Engineers: it is NO substitute for it.

Intended for all operatives and personnel in the electrical contracting industry, students and electricians, the book is full of practical advice, clearly explains the background to the design principles set out in the regulations and concentrates on the vital areas of earthing and bonding, protection and circuit design.

Electric Wiring: Domestic
by A.J. Coker
Revised by B. Scaddan
ISBN 0 434 90254 3
190 pages – 233 × 155 mm
Price £9.95

This ninth edition of Coker's *Electric Wiring: Domestic* remains the reliable guide to the practical aspects of domestic electric wiring it has been for close to half a century. It has been thoroughly revised by Brian Scaddan to take into account the latest amendments to the 15th edition of the *Regulations for Electrical Installations* issued by the Institution of Electrical Engineers, and modern techniques, practices and materials.

The book is thoroughly recommended to electrical contractors, installation engineers, technicians and students.

Op-amp Circuits Manual
by R.M. Marston
ISBN 0 434 91207 7
211 pages – 215 × 136 mm
Price £12.95

Operational amplifiers have become indispensable in many branches of electronics and this book shows how these devices may be readily used in modern electronic circuit design. Unlike many other authors, Mr. Marston clearly differentiates between the three basic types of opamp: standard (741, etc), Norton (LM3900, etc) and the OTA (operational transconductance amplifier) (CA3080, etc).

The emphasis of the book is on practical information and circuits that use modestly priced and readily available ICs and other devices.

The book should be of particular interest to the practical design engineer, technician, experimeter and student of electronics.

Heinemann Professional Publishing • Halley Court • Jordan Hill • OXFORD OX2 8EJ.

Digital Audio Projects
by R.A. Penfold
ISBN 0 85934 190 9
82 pages – 177 × 111 mm
Price £2.95

With the arrival of digital electronics in the audio engineering field, for instance,

compact disc players and digital tape recorders (DAT), there is undoubtedly a demand for suitable projects for the experimentalist. Unfortunately for them, as Mr Penfold says in the preface, "some types of digital audio equipment are probably not practical propositions for the DIY electronics enthusiast. CD player and DAT projects for the electronics hobbyist do not seem likely in the near future (if ever)". Although this reviewer does not agree with that statement, the book is nevertheless a worthwhile introduction to the theory and practice of digital audio.

More Advanced MIDI Projects
by R.A. Penfold
ISBN0 85934 192 5
118 pages – 177×111 mm
Price £2.95

When this book's predecessor, *MIDI Projects*, was published in June 1986, the Musical Instrument Digital Interface had been adopted by only a handful of electrophonic instrument manufacturers. That situation has changed radically in the few intervening years: MIDI sockets are now provided not only on most synthesizers, but also on many electronic pianos, electronic organs and not a few guitars, audio mixers, effects units, computers, and portable keyboards.

Since sales of electronic music instruments have never been better, this seems a suitable time for *More Advanced MIDI Projects*. Although "it is probably not possible for the amateur builder to compete with electronic instrument manufacturers", there are quite a few useful MIDI accessories that are well within the capabilities of the average electrophonics enthusiast. This book provides them!

Bernard Babani (publishing) Ltd • The Grampians • Shepehrds Bush Road • LONDON W6 7NF.

Guide to Broadcasting Stations
20th Edition
Edited by Philip Darrington
ISBN 0 434 90309 4
236 pages – 185 × 120 mm
Price £9.95

The latest update of this famous guide, which has been in print continuously since 1946, and has sold well over 300,000 copies since then, is again edited by Philip Darrington, former editor of *Electronic & Wireless World*.

The guide lists stations broadcasting world-wide in the long-, medium- and short-wave bands in frequency, geographical location and alphabetical order. It also includes much other useful information on such topics as choosing a short-wave receiver, aerials, writing reception reports, world time broadcasts in English, propagation, signal identification, and much more.

Students' Guide to Information Technology
by Roger Carter
ISBN 0 434 90222 5
233 pages – 215 × 138 mm
Price £8.95

This book is one in the HEINEMANN NEWNES INFORMATICS SERIES of textbooks covering the broad spectrum of IT topics for college-level students on BTEC, City & Guilds or professional courses with IT components, and for students of computer studies. 'Active learning' techniques have been incorporated, with achievement goals, case studies, and exercises applicable to a range of hardware and software.

The present work provides an overview of information technology. It includes an explanation of the microprocessor and the computer, an introduction to computer software, an account of audio and video technology as well as coverage of communications technology, and it gives the student an insight into office automation, into the use of IT in design and manufacturing, and into the significance of IT for our homes, our institutions, and for society at large.

Roger Carter is Reader in Information Technology at the Buckinghamshire College.

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BRITISH STANDARDS

BS7024:1988 (NEW) specifies the characteristics of 130 mm (5.25 in) flexible disk cartridges recorded at 7,958 ftprad 1.9 tpmm (48 tpi) on both sides using modified frequency modulation recording.

BS6789:1988 (NEW) is intended to specify all the additional functions and facilities that may be added to public switched telephone networks for use in conjunction with simple telephones or modems.

BS4584:Part 14:1989 (REPLACES BS4584 :Part 14:1977) specifies the requirements for properties of phenolic cellulose paper copper-clad laminated sheet, in thicknesses of 0.5 mm to 6.4 mm, for printed wiring boards.

BS5084:Part 4:1988 (REPLACES BS5084: PART 4:1974) – Magnetic tape for instrumentation applications – specifies the recording characteristics (including telemetry systems) interchange requirements.

Addendum No. 6 (1989) to BS3934:1965 specifies the dimensions of semiconductor devices and integrated electronic circuits.

All British Standards may be ordered from **The Sales Department • BSI • Linford Wood • MILTON KEYNES MK14 6LE.**

Readers should also note that each county in the UK has at least one large Public Library where complete sets of British Standards are held for general consultation

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The Homebuilt Dynamo
by Alfred T. Forbes
ISBN 0 9597749 0 4
182 pages – 308 × 215 mm
Price £42.00 (airmail post paid)

This is a fascinating book that has given your reviewer a few happy hours of browsing and absorbing ingenuity.

The book originates from the premise that there had to be a method of generating low-voltage electricity from mechanical energy and which could be developed from scratch in the average home workshop from (home-modified) off-the-shelf components and materials.

The systems of construction described were mainly worked out by trial and error. The result is a picture diary with over 300 illustrations detailing (with photos, schematics, and working drawings) the design and construction steps in the building of a low-voltage, low-speed, permanent magnet, three-phase alternator with built-in full-wave rectifier – which makes it, in effect, a DC generator.

The Homebuilt Dynamo (as wired in this book) can be used from 12 V to 36 V with a top rated output of 1000 watts – 28 A at 36 V at 740 RPM.

The machine has been specifically designed and simplified to the point where no soldering or welding is required. The use of connector strips (terminal blocks) for all wiring connections allows maximum experimentation and changing of components without a major hassle. Neither is there any foundry work, that is, no casting for the housing. There are no brushes to wear out.

The book also includes details of how to construct a precision diamond saw, a precision sheet metal cutter, a small lifting magnet, a foot-powered version of the Homebuilt Dynamo, a 139-pound flywheel, precision wire-winding jigs, and several pieces of apparatus for testing the magnets and the dynamo.

An absolutely marvellous book for the true experimentalist!

Todd-Forbes Publishing • P O Box 3919 •Auckland • NEW ZEALAND.

RGB-TO-CVBS CONVERTER RFK7000

This RGB-to-CVBS converter, designed by ELV GmbH, accepts digital as well as analogue RGB signals from computer systems, and supplies a composite output signal suitable for driving a monitor, a PAL-compatible TV set with SCART input, or a video recorder.

Nearly all of today's home computers and personal computers (PCs) are capable of supplying RGB (*red-green-blue*) output signals for driving a colour monitor. The RFK7000 RGB-to-CVBS (*chrominance-video-blanking-synchronisation*) converter allows computer-generated colour pictures to be recorded on a VCR, or displayed on a TV set, which normally has a greater screen size than a computer monitor. This brings interesting applications related to 'televised' demonstrations, multi-display networks, etc. within reach of the computer enthusiast with an interest for graphics applications.

Connecting the converter

The RFK7000 has 4 connectors on its rear panel:

BU1:
This socket accepts a 3.5 mm jack socket via which the unregulated 12 V d.c. supply voltage is applied to the converter.

BU2:
This SCART socket takes the 3 analogue RGB signals at an amplitude of about 1.5 V_{pp}. Analogue RGB signals allow an almost infinite number of colour combinations to be displayed.

BU3:
Via this SCART socket, the RFK7000 supplies the CVBS signal to the TV set or video recorder. A potentiometer allows the CVBS output level to be adjusted over a wide range.

BU4:
A 9-way sub-D connector accepts the digital RGB signals at TTL level supplied by the computer. The 3 signal lines and the associated Intensity line give a maximum of 16 colours.

The supply input of the RFK7000 is connected to a mains adapter with 12 V d.c. output. The SCART output is connected to the CVBS (composite-video) input of the video recorder, monitor or TV set. Either BU2 or BU3 is used to drive the RFK7000: BU2 for analogue, BU3 for digital, RGB sources.

Optimum picture quality is achieved by adjusting the VIDEO LEVEL control on the front panel of the converter.

Circuit description

The circuit diagram of the RFK7000 is fairly complex — see Fig. 1.

Digital RGB input

The digital RGB signals are applied tot he converter via 9-pin socket BU_4. This input is intended mainly for IBM PCs and compatibles equipped with colour graphics adapter (CGA). A CGA card supplies the 3 RGB signals plus an intensity signal that allows any basic colour to be switched to half intensity. This results in a maximum of 16 different colours. The pinning of the 9-way connector is as follows:

Pin 1: ground
Pin 2: not connected
Pin 3: red
Pin 4: green
Pin 5: blue
Pin 6: intensity
Pin 7: not connected
Pin 8: horizontal sync
Pin 9: vertical sync

The RGB and intensity signals are applied to XOR gate inputs (IC_4). Jumpers Br_1 and Br_2 enable the RGB and/or intensity signal to be inverted, so that the entire video signal can be inverted if desired.

The intensity signal is coupled into a matrix network via a CMOS switch. The second brightness level can be adjusted with preset R_{23}.

The 3 RGB signals are taken to the analogue inputs (pin 3, 4 and 5) of PAL encoder IC_7 (a Type MC1377) via a resistor network composed of R_{16}–R_{21} and R_{36}–R_{38}. At the chip inputs, the RGB signals have an amplitude of about 1 V_{pp} at maximum intensity.

Each synchronisation signal is first fed to a transistor buffer stage, T_1-T_2, and from there to a XOR gate in IC_6. The polarity of the synchronisation signals can be set to requirement with the aid of jumpers Br_3 and Br_4. XOR gate IC_{6b} supplies the composite sync signal at digital level. This negative-going signal is fed to pin 2 of IC_7 via voltage divider R_{39}-R_{40}.

PAL encoder

The Type MC1377 PAL encoder from Motorola forms the nucleus of the circuit, because it performs the bulk of the signal conversion functions. The colour subcarrier frequency is adjustable with trimmer C_{25}, while the position of the colour burst on the rear porch of the CVBS signal is adjusted with R_{34}.

Analogue RGB input

The circuit takes analogue RGB signals from SCART socket Bu_2. This is intended for computers such as the Atari ST or Commodore Amiga, having an analogue or quasi-analogue RGB output. Since the RGB output level supplied by these computers is usually 1.5 V_{pp} to 3 V_{pp}, potential dividers R_8-R_9-R_{10} and R_{36}-R_{37}-R_{38} are required to ensure that the converter inputs are driven with a maximum level of 1 V_{pp}.

The RFK7000 allows separate as well as composite sync signals to be applied to the SCART input. Separate horizontal syncs at pins 10 and 14 are fed to T_1 and T_2 via 4.7 kΩ resistors. The function of the transistors is similar to those used for the digital sync signals, as discussed above. A composite sync signal as supplied by, for instance, the Atari ST, is applied via pin 20 of the SCART input. This signal is peculiar because it lacks horizontal synchronisation pulses during the vertical blanking interval. The MC1377, however,

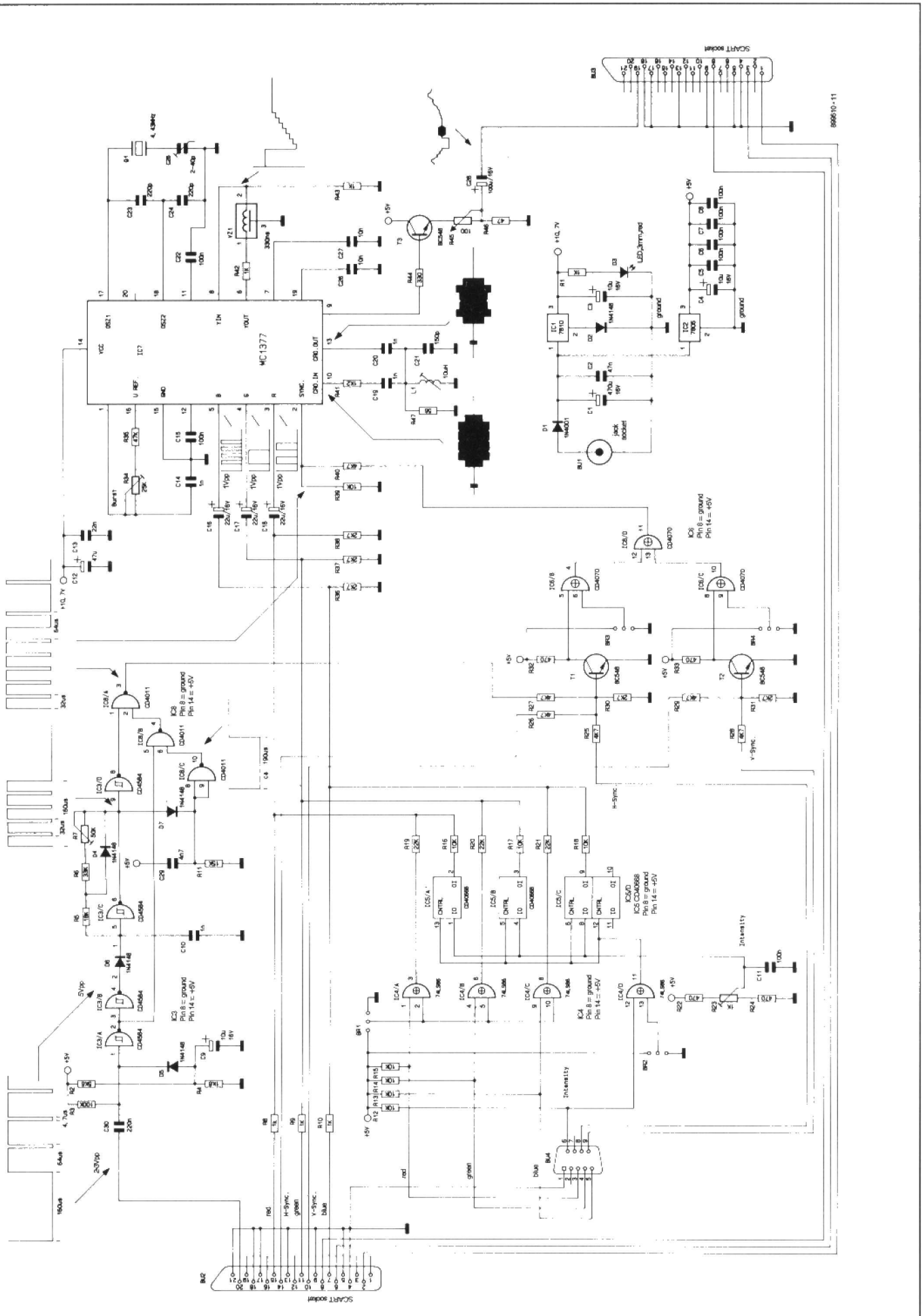
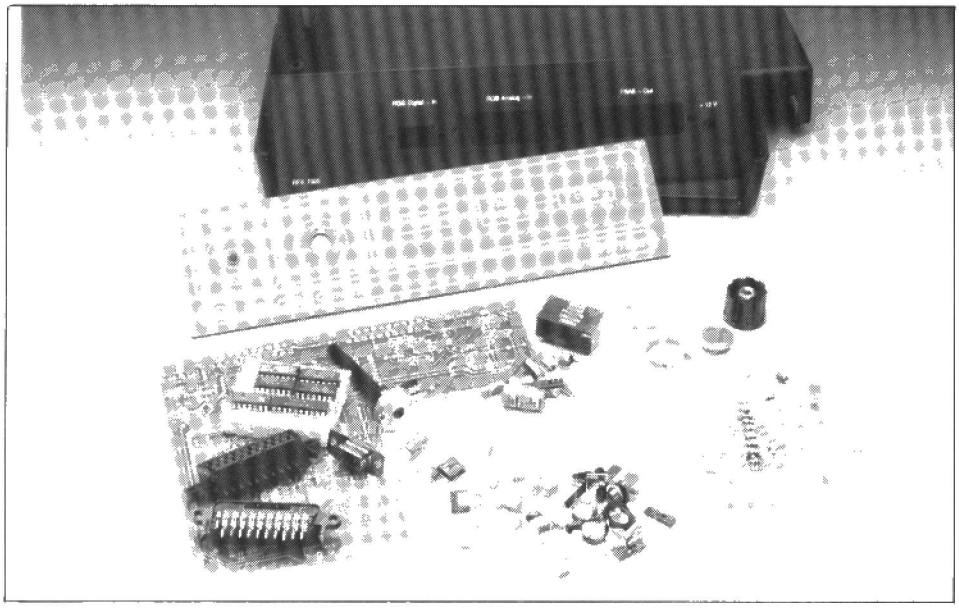


Fig. 1. The heart of the RGB-to-CVBS converter is formed by a PAL encoder Type MC1377 from Motorola.



Content of the kit supplied by ELV France.

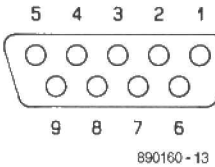
can not work properly without these pulses. The circuit around IC_3 and IC_8 converts the composite video signal into a standard composite sync signal that can be handled by the MC1377.

The composite synchronisation signal at pin 20 of the SCART input socket has an amplitude of 2 to 3 V_{pp}. A clamping circuit composed of C_{30}-R_2-R_3-R_4-D_5-C_9 is used to derive a direct voltage from the composite sync signal. This direct voltage is given a digital level to control gate IC_{3a}. A subsequent gate, IC_{3b}, inverts this control voltage.

Gate IC_{3c} and surrounding components C_{10}-R_5-R_6-R_7-D_4 form an oscillator that is disabled outside the vertical blanking interval by means of D_6. This means that the oscillator supplies horizontal synchronisation pulses during the raster blanking interval only. The number of pulses and with it their spacing (32 µs) is adjusted with preset R_7. Gate IC_{3d} normally supplies a steady logic high level, but positive-going horizontal sync pulses during the vertical blanking interval.

The length of the raster blanking interval is determined by components D_7-C_{29}-R_{11} and inverter IC_{8c}, whose output level changes from low to high at the end of the vertical synchronisation. This event enables the regenerated horizontal synchronisation pulses from pin 2 of IC_{3a} to be added via IC_{8b}, so that the output of the sync generator, pin 8 of IC_8, supplies a normal composite synchronisation signal.

If the input signals for the converter are obtained via SCART socket BU_2, the jumpers on Br1 and Br2 must be set in a

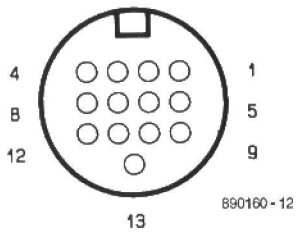


9-way sub-D video connector

front view

Pin	Signal
1	ground
2	ground
3	red
4	green
5	blue
6	intensity
7	n.c.
8	h-sync
9	v-sync

Fig. 2. IBM PC CGA socket pinning.



Atari ST 13-way monitor connector

front view

Pin	Signal
1	audio output
2	composite sync
3	port IO87; YM-2149 sound generator
4	monochrome sense
5	audio input
6	green
7	red
8	+12 V via 1k2
9	horizontal sync
10	blue
11	monochrome video
12	vertical sync
13	ground

Fig. 3. Atari ST monitor socket pinning.

Parts list

Resistors:
R_{46} = 47Ω
R_{44} = 330Ω
R_{22};R_{24};R_{32};R_{33} = 470Ω
R_1;R_8;R_9;R_{10};R_{42};R_{43} = 1k0
R_{41} = 1k2
R_4 = 1k8
R_{30};R_{31};R_{36};R_{37};R_{38} = 2k7
R_{25} – R_{29} = 4k7
R_2 = 5k6
R_{12} – R_{21} = 10k
R_{11} = 15k
R_5 = 18k
R_6 = 33k
R_{35} = 47k
R_3 = 100k
R_{45} = 100Ω potentiometer with 6 mm spindle
R_{23} = 1k0 preset H
R_{34} = 25k preset H
R_7 = 50k preset H

Note: R39, R40 and R47 are not fitted. R19, R20 and R21 changed w.r.t. circuit diagram.

Capacitors:
C_{21} = 150p
C_{23};C_{24} = 220p
C_{10};C_{14};C_{19};C_{20} = 1n0
C_{29} = 4n7
C_{26};C_{27} = 10n
C_{13} = 22n
C_2 = 47n
C_5 – C_8;C_{11};C_{15};C_{22} = 100n
C_{30} = 220n
C_3;C_4;C_9 = 10µ; 16 V
C_{16};C_{17};C_{18} = 22µ; 16 V
C_{12} = 47µ; 16 V
C_{28} = 100µ; 16 V
C_1 = 470µ; 16 V
C_{25} = 40p trimmer

Semiconductors:
IC_7 = MC1377
IC_8 = CD4011
IC_5 = CD4066
IC_6 = CD4070
IC_3 = CD4584
IC_4 = 74LS86
IC_2 = 7805
IC_1 = 7810
D_1 = 1N4001
D_2;D_4 – D_7 = 1N4148
D_3 = LED; red; dia. 3 mm
T_1;T_2;T_3 = BC548

Miscellaneous:
Q_1 = quartz crystal 4.433 MHz.
Vz_1 = 330ns delay line.
L_1 = 10µH, adjustable.
Br_1 – Br_4 = 3-way pin header.
BU_2;BU_3 = SCART socket for PCB mounting.
BU_4 = 9-way angled sub-D socket for PCB mounting.
BU_1 = 3.5 mm jack socket for PCB mounting.
4 off jumpers.
6 off screw M3×8 mm.
6 off nut M3.
Enclosure.
PCB Type ELV892525.

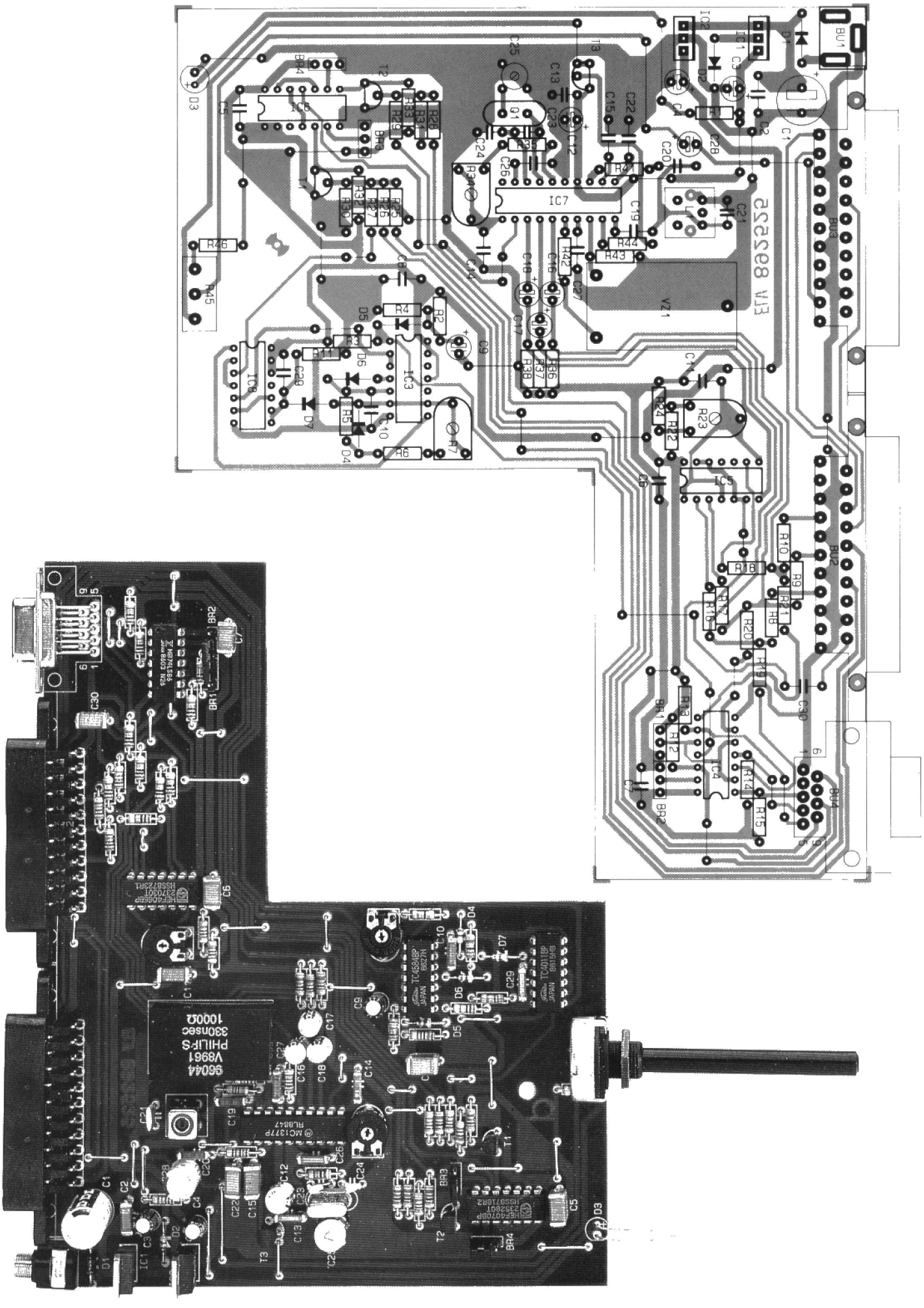


Fig. 4. Component mounting plan and top view of the printed-circuit board for the RGB-to-CVBS converter.

manner that ensures low levels at the outputs of XOR combination IC4 (Br1 and Br2 at +12 V).

CGA and 50/60 Hz

The colour graphics adapter (CGA) in IBM PCs and compatibles supplies a vertical scanning frequency of 60 Hz. Most modern TV sets are capable of detecting this and switch automatically from 50 Hz to 60 Hz. Older types, however, may require the vertical synchronisation to be corrected if the picture rolls. In most cases, this adjustment is fairly simple to make by means of the vertical sync control at the rear of the set.

In case the picture is not correctly centred, use MS-DOS command

MODE CO80,R

to shift the entire picture one character to the right.

Output circuit and power supply

The composite output signal is supplied by buffer T3, level control R45 and electrolytic capacitor C28.

The RFK7000 has two on-board voltage regulators, so that is conveniently powered from a standard mains adapter with 12 V d.c. output at about 300 mA. The unregulated input voltage is applied via 3.5 mm jack socket BU1, and fed to buffer capacitor C1 via D1, which affords reverse polarity protection. Capacitor C2 serves to suppress noise. Regulator IC1 has a diode, D2, connected to its ground terminal to raise the output voltage from 10.0 to about 10.7 V. This provides the supply voltage for the PAL encoder MC1377, which requires a minimum of 10.5 V for correct operation. Capacitor C3 serves to eliminate any risk of oscillation. LED D3 is powered via R1 and indicates that the RFK7000 is switched on. Finally, the 5 V supply for the digital circuits is formed by regulator IC2 in combination with decoupling capacitors C4 to C8.

Construction

The RFK7000 is relatively simple to build because all parts are accommodated on the single printed-circuit board supplied with the kit. Construction is expected to take about 3 hours.

Start by inserting the lowest profile parts, the 29 wire links (do not solder them as yet). Next, bend all resistor terminals to obtain the right pitch. Insert the resistors in accordance with the Parts List and the component overlay on the PCB. Push the terminals apart after inserting the resistors to ensure that they do not drop from the board as it is turned and pushed firmly on a flat surface. Solder all wire terminals, and cut them off as close as possible to the solder joint.

Next, turn the board and fit the 7 diodes, 8 ICs, capacitors, etc. in the normal manner. Lastly, mount the 4 connectors and the video level potentiometer on to the board. Check your work by inspecting all solder joints.

Remove the nut from the 3.5 mm jack socket, and fit the rear panel of the enclosure on to the rear side of the PCB. The two SCART sockets and the 9-way sub-D socket are each secured with two M3×10 mm screws inserted through the socket flanges from the outside of the rear panel. Each screw is secured with two M3 nuts. Mount and tighten the nut on to the jack socket.

The front panel supplied with the kit is also quite simple to mount. Remove the nut from the level control potentiometer, mount the front panel, and secure the nut again at the outside. The potentiometer spindle is cut to about 10 mm. Next, fit the collet knob and secure it on to the spindle.

Insert the PCB with the front and rear panel attached into the guides in the bottom half of the enclosure.

Jumper settings

Most CGAs in IBM PCs and compatibles supply a positive h-sync and v-sync signals. Some cards, however, supply a negative v-sync signal.

The horizontal sync signal is fed to the base of T1 via pin 8 of socket BU4 and R25, and the vertical sync signal to the base of T2 via pin 9 of BU4 and R28. Assuming that positive sync signals are applied, either the horizontal or the vertical sync signal must be inverted to ensure a negative-going composite sync signal at pin 11, the output of IC6d. This may be achieved in two ways:

1. Pin 6 of IC6b is tied to +5 V via Br3, and pin 9 of IC6c to ground via Br4;
2. Pin 6 of IC6b is tied to ground via Br3, and pin 9 of IC6c to +5 V via Br4.

Since most CGA cards supply positive-going RGB signals, Br1 is connected to ground to ensure that the signals are not inverted by gates IC4a through IC4c. The same applies to the intensity signal: pin 13 of IC4d is normally connected to ground via Br2. The value of R23 determines the effect of the intensity bit on the colours, and may be adapted to individual requirements.

The jumpers on the board are fitted to allow the RFK7000 to accept sync polarities from CGA cards other than the standard types around. In case of doubt, consult the manual supplied with your CGA card.

Alignment

The alignment of the RGB-to-CVBS converter concentrates mainly on PAL encoder IC7. Alignment is straightforward, and can be carried out without an oscilloscope.

Apply a digital RGB signal to BU4 (if necessary, refer to the pinning shown in Fig. 2), and connect a monitor with CVBS input to BU3. Adjust C25 and R34 alternately until the colour appears on the monitor.

Alignment with the aid of an oscilloscope is even simpler because the instrument allows R34 to be adjusted beforehand. Connect the scope to the output of the RFK7000, pin 19 of BU3. Adjust R34 until the colour burst starts at 0.5 µs after the horizontal sync pulse.

Next, adjust the cross-colour filter, L1-C21. Use an insulated trimming tool to adjust the core of L1. Watch the picture on the monitor, and minimize the moving cross-colour patterns that occur typically at colour boundaries. This adjustment is also possible with the aid of an oscilloscope: peak the chrominance signal measured at pin 10 of the PAL encoder chip. This completes the adjustment of the RFK7000 for use with CGA-compatible PCs.

No further alignment is required if the separate sync signals are applied to the SCART input socket. If, however, composite sync is applied to pin 20, preset R7 has to be adjusted.

Although the Atari ST supplies separate sync signals to the monitor socket (pinning: see Fig. 3), composite sync is used on the SCART cable provided with some STs.

Preset R7 is used to set the pulse spacing of the horizontal sync signal generated during the vertical blanking interval. The pulse spacing may be measured at pin 8 of IC3d, and should be about 32 µs. The actual value is fairly uncritical — the important thing is that the MC1377 receives an even number of horizontal sync pulses during the raster blanking interval. This is required for correct synchronisation of the internal PAL bistable. Constructors not in possession of an oscilloscope simply adjust R7 until the colour shows up on the screen. Some re-adjustment of R34, R7 and C25 may be required for optimum results, because these adjustments have a fairly large range and some interaction. In most cases, however, the alignment of the RFK7000 is straightforward by optimising the colour fidelity with the aid of the monitor.

Finally, it should be noted that the graphics card or computer used to drive the converter must be programmed to supply 50 Hz vertical synchronisation pulses if pictures are to be recorded on a VCR. This is not required for most monitors and TV sets, whose vertical scanning rate is adjusted either automatically or manually to synchronize at 60 Hz. The RFK7000 is not suitable for NTSC systems.

A complete kit of parts for the RGB-to-CVBS converter, which is designed in West-Germany, is available from the designers' exclusive worldwide distributors (regrettably not in the USA and Canada):

ELV France
B.P. 40
F-57480 Sierck-les-Bains
FRANCE
Telephone: +33 82827213
Fax: +33 82838180

Also see ELV France's advertisement elsewhere in this issue.

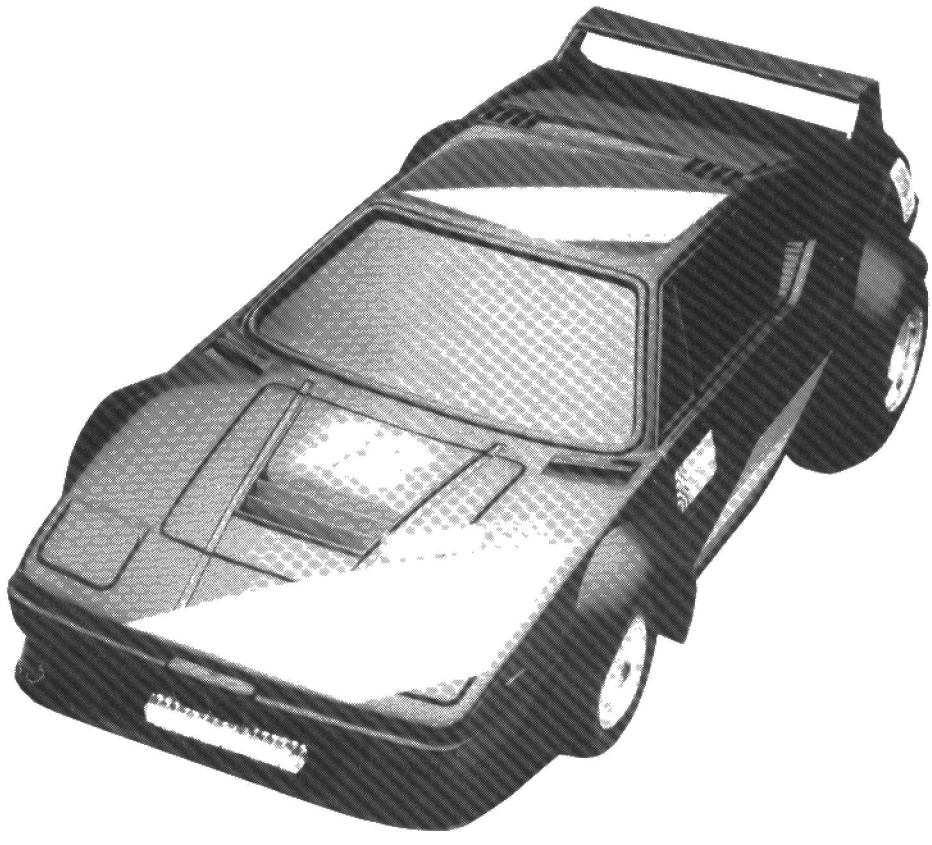
INTERMEDIATE PROJECT

A series of projects for the not-so-experienced constructor. Although each article will describe in detail the operation, use, construction and, where relevant, the underlying theory of the project, constructors will, none the less, require an elementary knowledge of electronic engineering. Each project in the series will be based on inexpensive and commonly available parts.

6. 16-channel running lights

W. Werner

This month we turn our attention to a less serious design. The robots in the popular TV series 'Battlestar Galactica', and the super-intelligent car 'Kitt' in 'Knight Rider' are credited with seeing abilities obtained from an electronic eye. The running lights circuit described here simulates such a scanning eye, and is aimed at our younger readers, the budding 'Knight-Riders' and model robot constructors.



The circuit diagram of Fig. 1 shows that the anodes of the 16 LEDs that simulate the scanning eye are commoned and connected to the +12 V supply via R1. We can make any 1 of the 16 LEDs light by connecting its cathode to the negative supply rail, which is the same as ground in the present case. Circuit IC3 is the electronic equivalent of a single-pole 16-way rotary switch because it takes the cathode connections to ground in a sequential manner. Only one LED lights at a time. First, output S0 goes low, then S1, then S2 and so on, to S15. Upon reaching S15, the 'switch' is turned back again to S14, S13, and so on, down to S0.

Each LED connected to IC3 can be thought of as having a number between 0 and 15. This number is applied in binary coded decimal (BCD) form to inputs D1–D4 of IC3. This should make the type description of the IC, *4-to-16 decoder*, clear: the device converts the 4-bit code applied to D1–D4 into the corresponding decimal number, 0 through 15. Since only one output is active (that is, logic low) at a time, the description *1-of-16 decoder* may also be used.

With 4 digital selection inputs, $2^4 = 16$ channels can be addressed individually. Output channel 0 (IC3 terminal S0) is actuated by binary code 0000, and output channel 15 (IC3 terminal S15) by binary code 1111. Table 1 lists all intermediate values, and shows the 'walking zero' in the output line configuration. Control input D1 changes state at the highest rate (0-1-0-1, etc.), and is therefore called the *least-significant* (LS) address line. Control input D4 changes state at every eighth transitions of D1. In the present 4-bit system, it is therefore the *most-significant* (MS) address line.

Counter and clock generator

The 1-of-16 decoder/LED driver is addressed by a counter, IC2. This IC contains 4 series-connected bistables. Each of these divides its input frequency by 2, and supplies its output signal at a pin designated Q. Since there are 4 internal bistables, outputs QA through QD can take on 16 different logic configurations.

The clock signal applied to input CLK of IC2 is divided by 2 in the first internal divider, which is associated with output QA. The clock signal divided by 4 appears on output QB, divided by 8 on QC, and divided by 16 on QD. This means that QA

changes at the highest rate, so that it can be connected to input D1 of the LED decoder, IC3. Similarly, MS output bit QD of the counter changes every 8 transitions of QA, so that it can be used for driving the MS address input of the LED decoder. The operation of the counter is illustrated by the timing diagram of Fig. 2.

Input U/$\overline{D}$ allows the counter chip to be programmed to count up (0 to 15; U/$\overline{D}$=1) and down (15 to 0; U/$\overline{D}$=0). The bistable built from NAND gates N2 and N3 ensures that the count direction is reversed automatically when state 0 or 15 is reached.

Pin 8 of gate N3 functions as the SET input of the bistable, and pin 6 of N2 as the RESET input. Pin 10 of N3 forms output Q, and pin 4 of N2 output $\overline{Q}$. The logic state of Q is always complementary to that of $\overline{Q}$. Output Q goes high when the bistable is set, and $\overline{Q}$ when the bistable is reset. In the present circuit, only output Q is used. A logic 0 at pin 8 of N3 causes the bistable to be set, and output Q to go high. Output Q is made low again by a logic 0 at pin 6 of N2.

The circuit diagram shows that the bistable is set and reset by the logic low levels supplied by LED decoder outputs S0 and S15 respectively. When S0 goes low (D1 lights), it simultaneously causes the NAND bistable to be set, so that counter control input U/$\overline{D}$ is made high. As a result, the counter starts to count up from state 0. Similarly, when S15 goes low (LED D16 lights), U/$\overline{D}$ is pulled low, so that the count direction is reversed.

Inputs A through D of counter IC2 are *jamming-inputs* that enable a preset value to be loaded when input PE (preset enable) is made logic high. Since the counter is to start at state 0000, all 4 jamming inputs have been tied to ground. Components C2 and R3 briefly take the PE input high at power-on, causing the counter to load '0000' as the preset value.

The CI (carry in/clock enable) of the counter is made permanently low to enable the counter to work continuously. Counting is halted, and the current output state is frozen if CI is taken high. This option is not required here, however.

Count mode input B/$\overline{D}$ (binary/decade) of IC2 is connected to +12 V because binary counting is required.

The clock signal for the counter is provided by Schmitt-trigger NAND gate N1 and frequency-determining components C1-R2. Together, these parts form an oscillator.

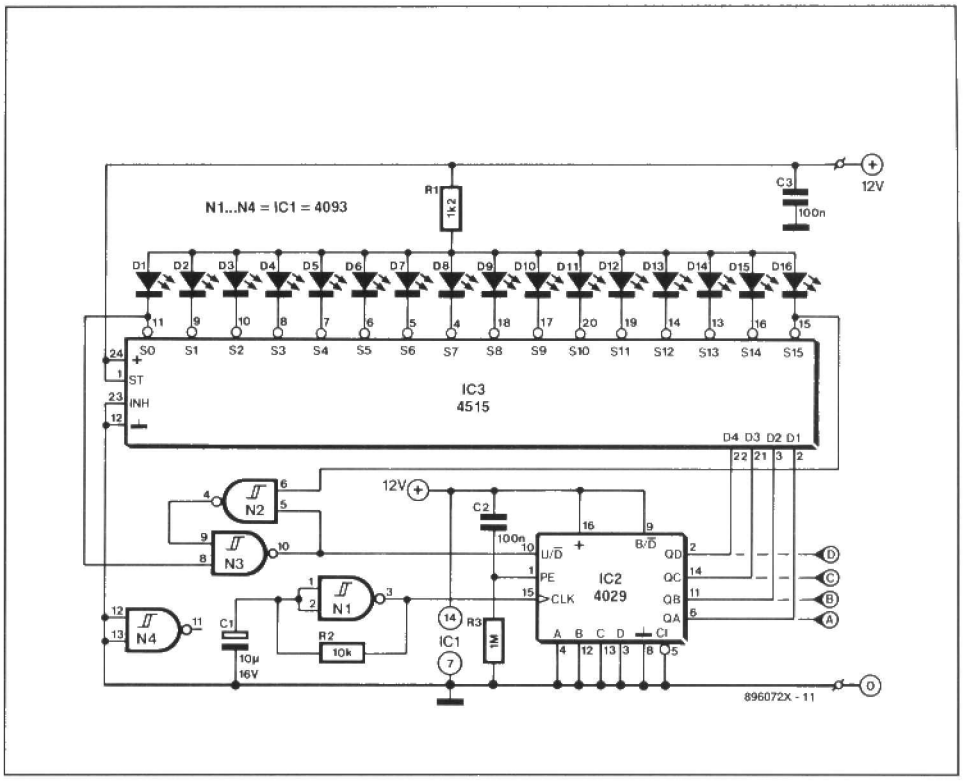


Fig. 1. The circuit is essentially composed of a 1-of-16 decoder/LED driver (IC3), a counter (IC2), and a clock generator (gate N1).

Construction

The present circuit is probably too com-

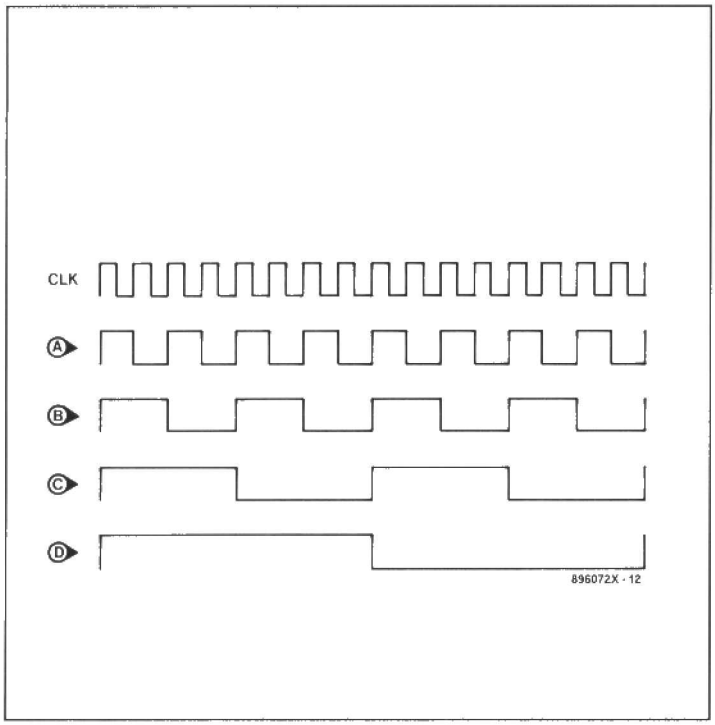


Fig. 2. Timing diagram illustrating the operation of counter IC2, which is composed of four cascaded bistables.

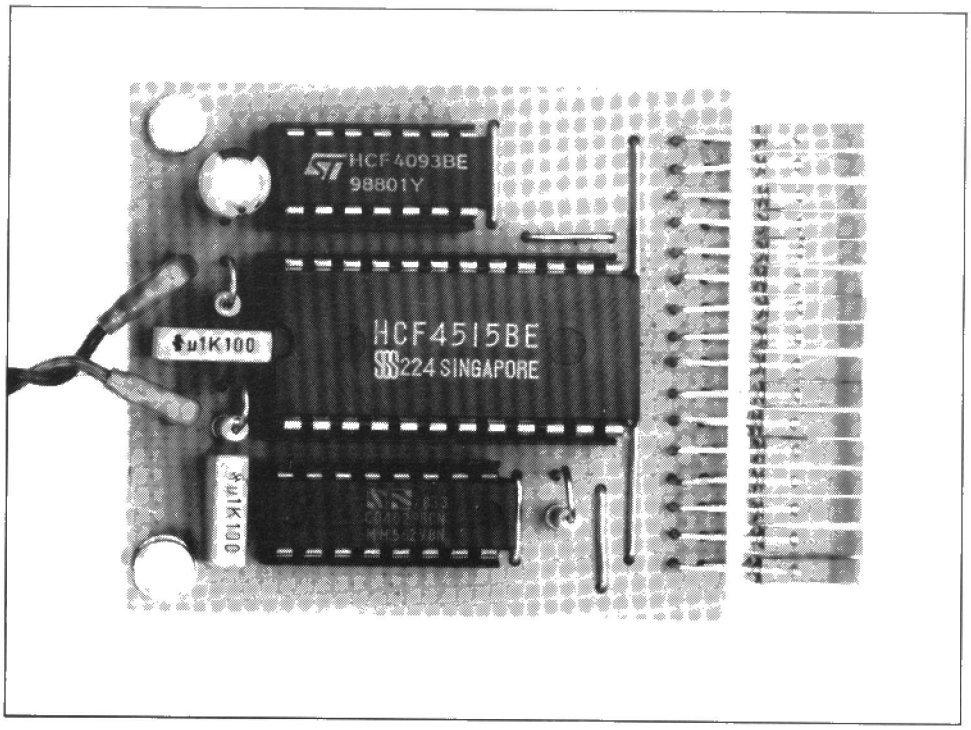
decimal	binary	1-of-16 code
	D4–D1	S0 S15
0	0000	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1	0001	1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1
2	0010	1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1
3	0011	1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1
4	0100	1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1
5	0101	1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1
6	0110	1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1
7	0111	1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1
8	1000	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
9	1001	1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1
10	1010	1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1
11	1011	1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1
12	1100	1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1
13	1101	1 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1
14	1110	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1
15	1111	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

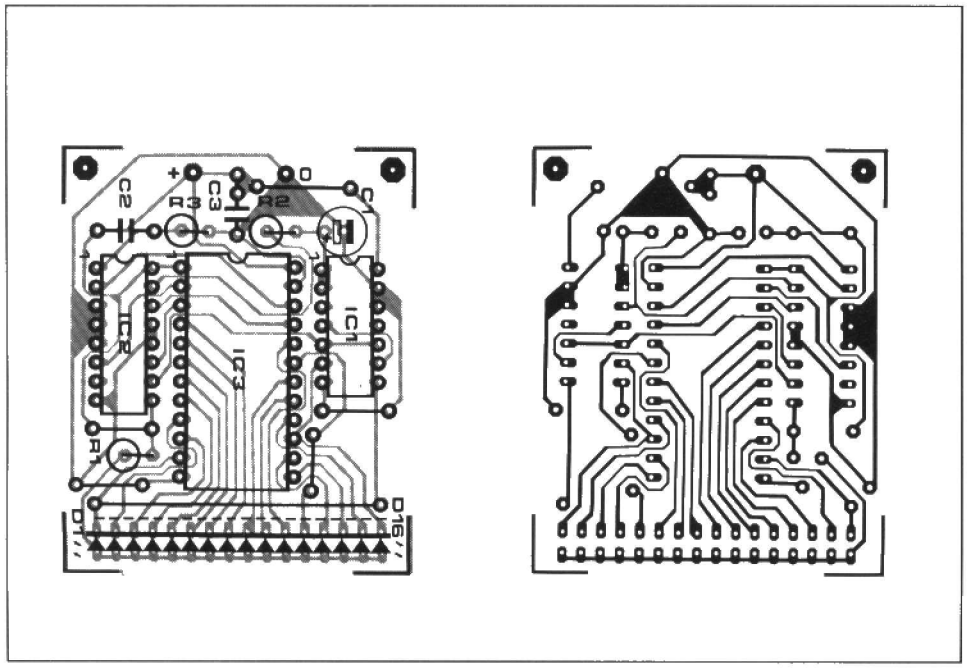
Table 1. Relation between the binary input and 1-of-16 decoded output of decoder IC3. Note the 'walking zero' in the output states.

plex to build on a Universal Prototyping Board as used for other projects in this series. The lay-out of a suitable printed-circuit board is, therefore, given in Fig. 3.

Refer to the Parts List when selecting the components. First mount the wire links, then the resistors, capacitors and IC sockets. The LEDs are fitted last. The introductory photograph illustrates the use of 16 rectangular LEDs whose terminals have been bent at right angles. Round LEDs are, of course, also suitable, and the constructor is left free to decide on the most realistic appearance of the electronic eye. Use a transparent red bezel in front of the LEDs to improve the visibility.

Although the supply voltage of the running lights is given as 12 V, the circuit also works fine when powered from a 9 V or 5 V source. Some experimenting with the value of R_1 and/or C_1 may be required, however, to obtain the desired scanning rate at relatively low supply voltages. Also, as a general rule, make R_1 smaller with low supply voltages to ensure sufficient LED brightness.





Parts list

Resistors:
R_1 = 1k2
R_2 = 10k
R_3 = 1M0

Capacitors:
C_1 = 10µ; 16 V; radial
C_2;C_3 = 100n

Semiconductors:
D_1 – D_{16} = LED; red; rectangular
IC_1 = 4093
IC_2 = 4029
IC_3 = 4515

Miscellaneous:
PCB 896072 (not available through the Readers Services).

Fig. 3. Printed-circuit board for the running-lights circuit.

ELECTRONICS SCENE

World's first single-chip teletext decoder

Plessey's new Type MV1815 is claimed to be the world's first single-chip teletext dedoder. The device, manufactured in the company's advanced 1.4 micron CMOS process, also incorporates a data slicer, dual acquisition circuitry and RGB display logic.

With the MV1815, a complete teletext system can be built with just the addition of a single dynamic random-access memory (DRAM) chip. Depending on the size of the memory, up to 254 pages of text can be stored for intermediate access by the viewer. Most currently marketed systems allow storage of only 4 pages.

The new MV1815 supports several languages on the single chip, and is capable of receiving all packets 0 to 31. All 'Level-1' teletext functions are incorporated on chip, plus many 'Level-2' features. The new Plessey device is claimed to have improved graphics capability and greater programming flexibility over competitive products.

Plessey Semiconductors Ltd • Cheney Manor • Swindon • Wiltshire SN2 2QW. Telephone: (0793) 36251. Fax: (0793) 36251 ext. 2198.

ANALOGUE-TO-DIGITAL CONVERSION TECHNIQUES

by Julian Nolan

The rapid growth in the digital sector of the electronics market has given rise to continued demands for more and more increases in the resolution and conversion speed of digital-to-analogue and analogue-to-digital converters. In spite of the industry meeting these demands, the selling price of all types of device has continued to fall. This is particularly true for medium speed/resolution flash devices: an 8-bit, 30 MHz type, for instance, is now available in quantity for well under £20. Advances in the digital-to-analogue converter field have been typified by higher specifications rather than lower prices.

Three main analogue-to-digital (A-D) conversion techniques are in common use: successive approximation, flash and integrating conversion.

Successive approximation has the advantage that for an n-bit converter only n number of stages are necessary in the successive approximation register (SAR), which makes this technique ideal for applications that require high resolution or low cost or both. The technique is illustrated in Fig. 1.

Initially, all output bits of the SAR are set to zero and then each bit, starting with the most significant, is set provisionally to one. If the output of the converter does not exceed the input signal voltage, the bit is left at one, otherwise it is reset to zero. From this, it is clear that an n-bit converter will require only n such conversion steps. This makes this type of converter relatively fast in comparison with those that use other techniques like single- or dual-slope integration.

Should the input voltage be altered during the conversion process, the resulting error will be no larger than the change during that time. Noise spikes, however, can cause totally erroneous output and must be avoided at all costs.

In general, it is advisable to use a sample-and-hold device in conjunction with this type of converter.

Typical conversion times range from 1 µs to 50 µs, while accuracies of 8–16 bits are available.

Flash conversion requires 2^n-1 comparators, thus limiting the resolution that can be achieved with this technique. Current IC fabrication technology permits up to 12 bits.

Two typical flash devices are Analog Devices' AD770 (8 bits at 200 MSPS) and TDC1020 (10 bits at 20 MSPS).

The technology relies more on 'force in numbers' than subtle design techniques at component level. As shown in Fig. 2, a reference voltage is applied to a resistive divider, whose equispaced outputs are applied to $n-1$ voltage comparators. The Gray-code output from the comparators is encoded by the priority encoder to form a usable binary output. Typical conversion rates vary from 10 MSPS to 500 MSPS, while resolutions of up to 12 bits are currently available.

Resolutions above 16 bits are generally the domain of integrating converters. These offer good linearity and resolutiuon while maintaining a reasonable cost/performance ratio. Typical applications include digital voltmeters, data acquisition systems, weighing and medical systems where the slow conversion rate inherent in these converters is not significant. An example of integrating conversion, dual slope, is shown in Fig. 3.

Initially, switch S1 is closed by the control logic. Switch S4 is then opened and the input voltage integrated for n clock periods, where n is usually the maximum count of the counter. At the end of this time, the integrator voltage, V_o, is

$$V_o = -V_{in} n T_c / RC \qquad [1]$$

where T_c is the clock period.

During this period, the polarity of the

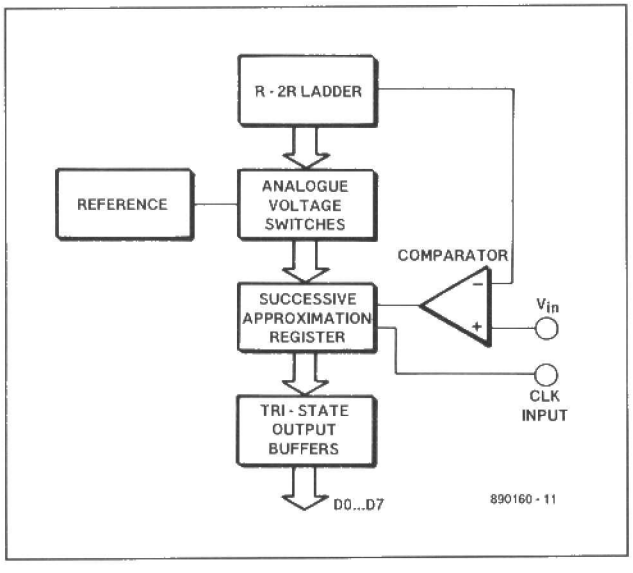


Fig. 1

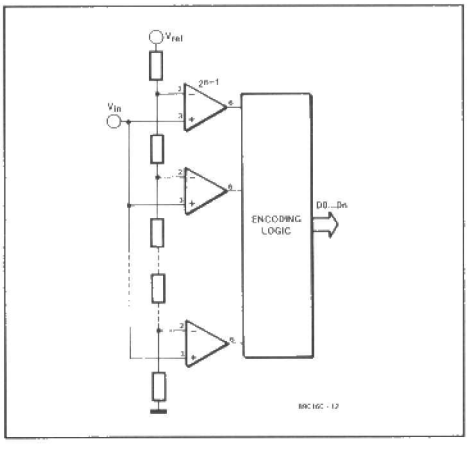


Fig. 2

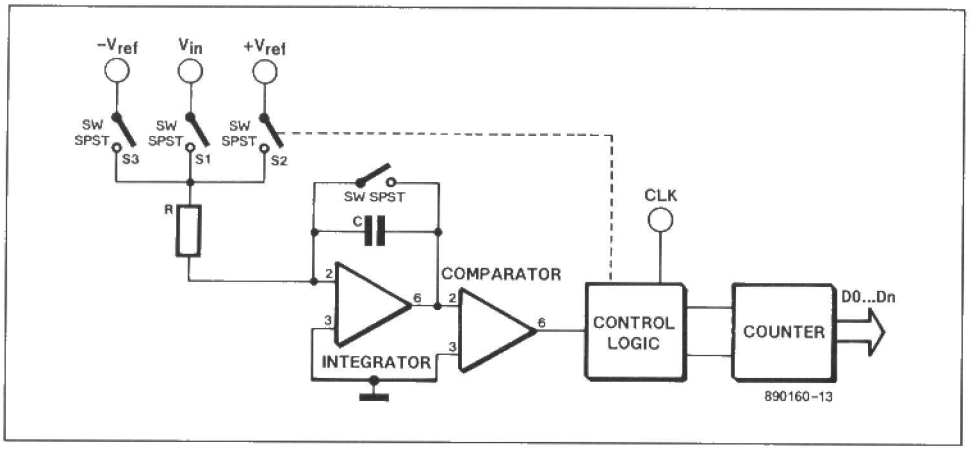


Fig. 3

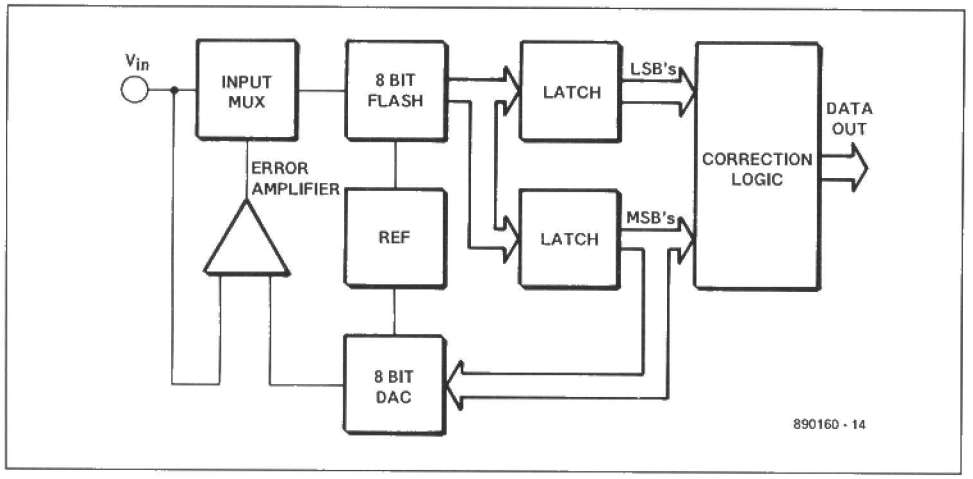


Fig. 4

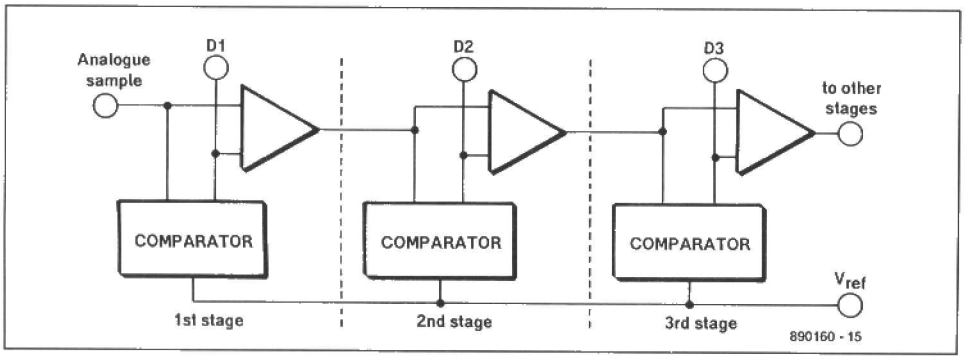


Fig. 5

input signal is detected by the comparator. At the end of the integration period, S1 is opened and, depending on the polarity of V_{in}, either S2 or S3 is closed to connect the integrator to the reference voltage that has a polarity opposite to that of V_{in}. Next, the counter is clocked from zero until the integrator output reaches 0 V: the output of the comparator then changes state and the count is stopped. Since integration takes place over the voltage range V_o,

$$V_o = -V_{ref} nx/RC, \quad [2]$$

where nx is the count reached by the time the integrator output passes zero.

Combining and rearranging [1] and [2] gives

$$nx = V_{in} / V_{ref} \quad [3]$$

Since n and V_{ref} are both fixed, the output count is directly proportional to the input voltage. Because both the first and the second integration occur under identical circumstances, the converter is not affected by any long-term variations in T_c, R or C, as confirmed by the disappearance of these terms from equation [3].

The major factors affecting the stability of the converter are:

(1) the stability of V_{ref};
(2) drift in integrator and comparator opamps;
(3) the stability of the 'on' resistance of S1 and S3.

Other techniques of integrating conversion are available, such as single-slope integration and charge balancing. These methods are relatively slow, however, and their use is restricted to applications that can support their relatively high conversion times.

As is seen, none of the three methods discussed provides both a high resolution and a high conversion speed. Where these are required in combination, say, 16 bits at 2 µs, use is made of subranging techniques, which are normally based on a single high-speed flash A-D converter as shown in Fig. 4.

In practice, these types of device are implemented in hybrid form. Some suffer from a reduced signal-to-quantization noise ratio at relatively high input frequencies, although those are not uncommon in A-D converters.

Initially, the input is sampled by the track and hold circuit. Subsequently, the most significant portion of the signal is converted by feeding the output word into a fast, highly accurate D-A converter, whose output is subtracted from the input. The resulting residue is converted to digital form at high speed and combined with the results of the earlier conversion to form the output word. Owing to the very high performance this technique demands from the adder and DAC, it is usual to incorporate some sort of error correction: a commonly encountered type is digitally corrected subranging (DCS). In this, the two bytes are combined in a manner that corrects the error of the LSB of the most significant byte. With the use of, for instance, an 8 and 5 bit conversion, an accuracte, high-speed 12-bit converter may be configured, although it should be noted that the resolution of the D-A converter must be greater than the resolution required to maintain conversion accuracy.

Future developments

Digital error correction, using a variety of techniques, from integrating to subranging, is now being introduced into a wide range of devices. This trend is likely to continue and, with the ever decreasing cost of data conversion products, will become increasingly relevant to the low-cost end of the market.

As regards conversion techniques, the serial converter or cascaded encoder as shown in Fig. 5 may well make a come back. First used in the 1960s as a method of A-D conversion, the serial converter is based on a number of comparators, each taking the residue of the previous stage and comparing it to a reference voltage. If the input is higher than the reference, a 1 is produced at the output, and the residue of the original input signal is subtracted

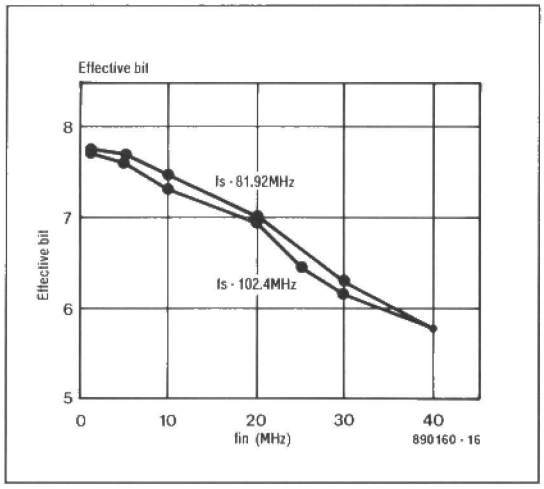


Fig. 6

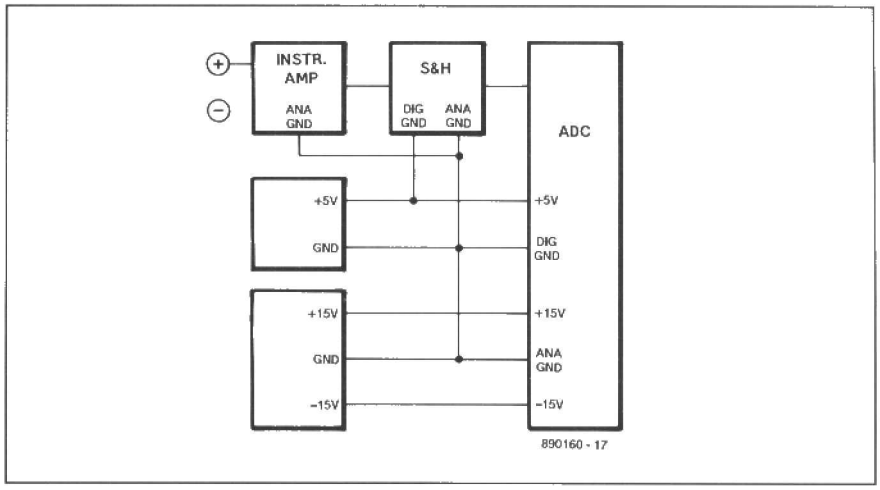


Fig. 7

from the reference and passed on to the next stage. If the input does not exceed the reference, the signal is passed to the next stage unaltered. It is usual to incorporate a ×2 amplifier to enable the use of a single reference voltage and restrict problems with noise.

In practice, this system has provided difficult to implement owing to errors introduced by the comparators and amplifiers, noise and also poor transfer characteristics in high-speed systems. With the advent of high-performance analogue components, however, some manufacturers are reconsidering this technique, since it offers a unique blend of speed, resolution, and low component count – at least in theory.

Design considerations

The effective resolution at a specified input frequency is usually not quoted in the manufacturers' data sheets and can often be well below the stated optimum. A graph of the SNR/effective number of bits vs the input frequency of an 8 bit, 100 MHz sampling A-D converter with a bandwidth of 40 MHz from a well-known manufacturer is shown in Fig. 6.

It is seen that at an input of 40 MHz and a sampling rate of 102.4 MHz, the effective resolution is about 6 bits. That means that only 64 possible output states are provided instead of the 256 that would have been available if the full 8-bit resolution had been maintained.

For applications that require a specified resolution to be maintained over the greater part of the input frequency, it is well worth considering, in situations that are not cost critical, over-specifying the AD converter to meet the requirement.

Although problems are evident in AD converter applications below 12 bits, most occur with accuracies of 12 bits or more, or with high-speed systems, where the problems are accentuated at higher resolutions.

If successive approximation is chosen for the A-D conversion, a sample-and-hold stage is essential and this may be a source of trouble in itself. Increasingly, however, some manufacturers, such as Datel in their 12-bit, 500 kHz ADS-111, are incorporating a S&H in the A-D converter package. However, there may be advantages, such as a reduction in cost or an improved specification, in using a separate S&H stage.

Three main building blocks are contained in a S&H stage: a capacitor, an analogue switch and a buffer amplifier. Some require an external hold capacitor, which must be chosen with great care as regards its dielectric absorption properties. Teflon or polystyrene capacitors, whose dielectric absorption is fairly small, are well suited to this purpose.

If the sampling system is used as the front end in an FFT system, particular attention should be paid to the aperture uncertainty and aperture time. The time should be chosen so that at the highest frequency the component does not change by more than one bit in the allotted time. It should also be noted that the S&H will always add errors to the A-D converter owing to effects such as non-linearity of the S&H off-set.

The use of a sin gle package containing the AD converter and the S&H has the advantages that some of the problems mentioned are minimized and noise may be less of a problem, especially in high-resolution systems.

Apart from the Datel device already mentioned, some other single-package units are the Sipex HS9474 and Analog Devices AD1332 (which includes an anti-

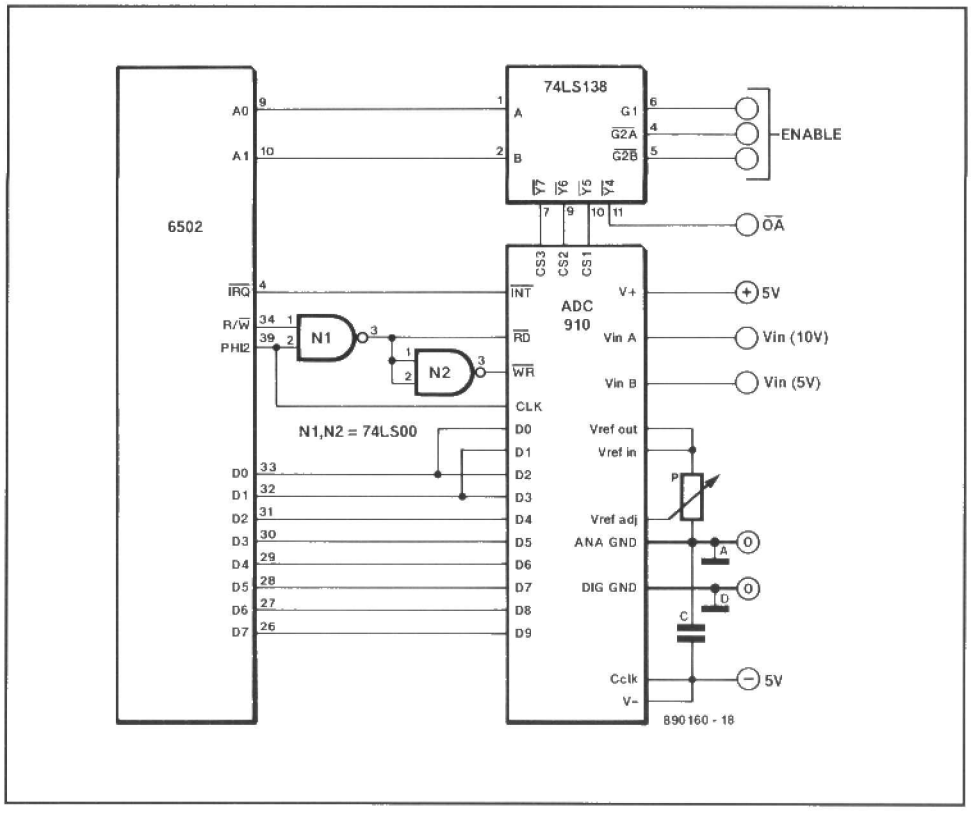


Fig. 8

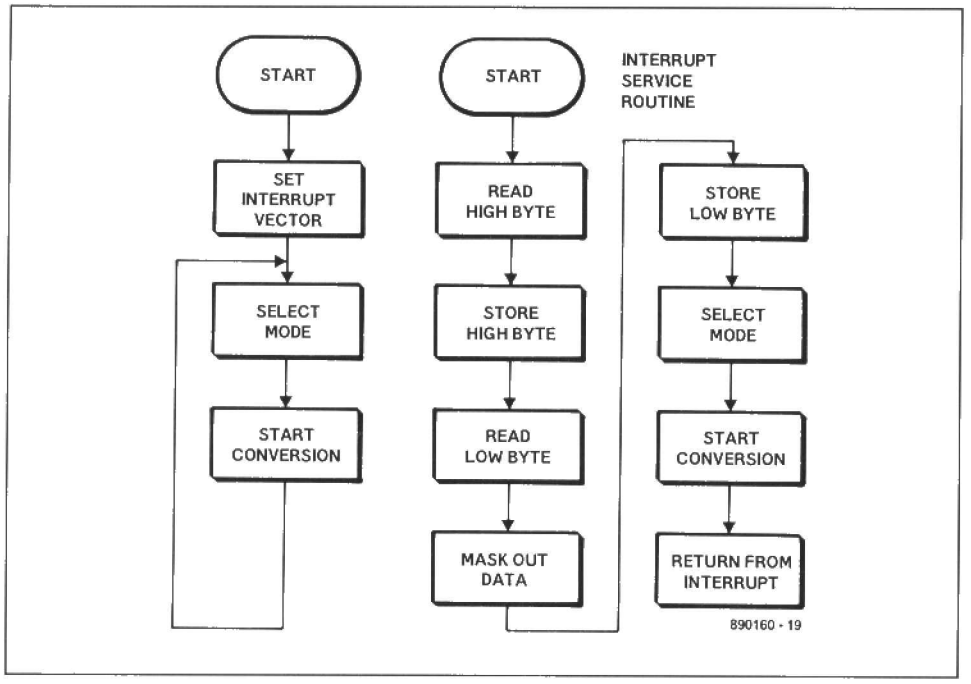


Fig. 9

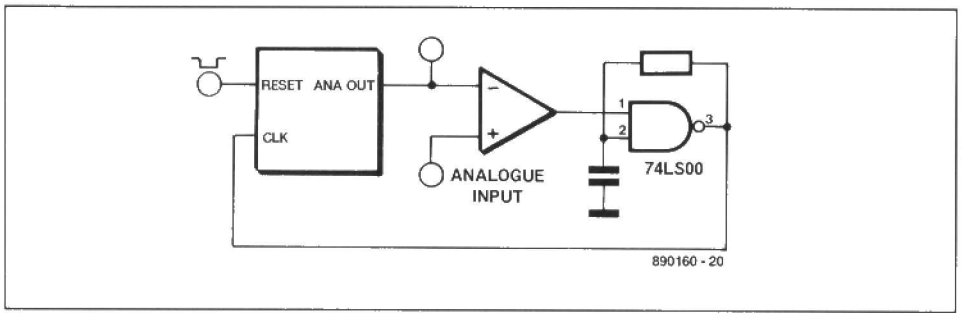


Fig. 10

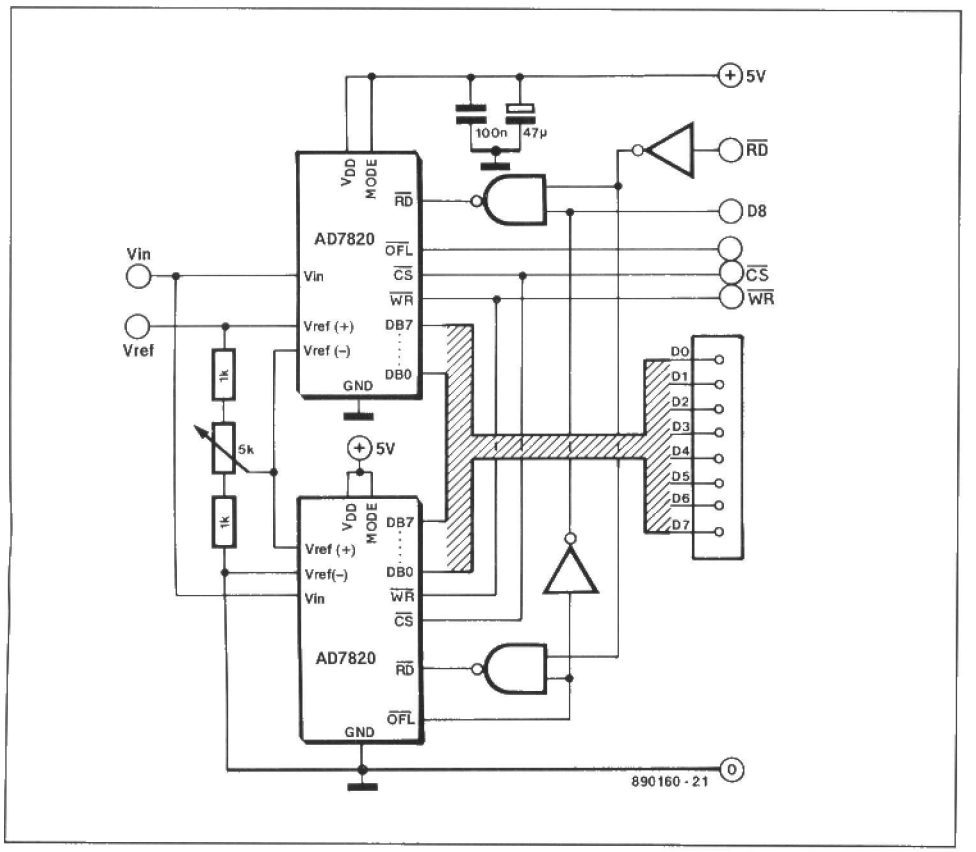


Fig. 11

aliasing filter).

Whatever technique is used, the analogue input section is vital to the operation of the converter, and usually includes one or more references in addition to conversion technique specific components like comparators and DA converters.

In ratiometric conversion, the reference is usually external and variable. In general, an on-chip reference usually helps to minimize noise, but in a number of cases advantages may be obtained from an external reference.

It is worth noting that the current-switching action of the D-A converter, at the typically fast clock rates used in successive approximation converters, may disturb the output of the analogue signal source, especially if it is a high-precision opamp,with a low slew rate. In that case, buffering will be necessary.

Design techniques

Whereas digital circuits may have noise margins of a few hundred millivolts, there is no room whatsoever for noise in analogue circuits. For instance, a 12-bit resolution A-D converter with a full-scale range of 3 V has a 0.5 LSB corresponding to 0.61 mV.

Power supplies are among the major sources of noise: the output of switch-mode types may have a noise level of more than 100 mV. Although the ability of an A-D converter to suppress DC supply changes, such as long-term drift (expressed as the power supply rejection ratio – PSRR), is usually good, HF noise is normally not suppressed to any great extent. Wherever possible, the supply voltages for the analogue section should be provided by a linear supply and bypasssed direct at the A-D converter. A multi-layer capacitor in parallel with a tantalum capacitor provides a suitable bypass.

To avoid ground loops, it is advantageous to have a 'star point' as close to the AD converter as possible – see Fig. 7. All ground lines should be of low impedance, necessitating wide ground tracks on the PCB or, preferably, particularly if double-sided or multi-layer boards are used, a separate ground plane underneath the AD converter package. In some cases, shielding the converter package from the top may be necessary.

Unless the analogue signal is free of noise, there is little point in taking the protective measures mentioned. To reduce the noise, suitable filters and shielded cables should be used.

Applications

Some of the factors worth considering when choosing an A-D converter for a particular application are:

- type of converter;
- required conversion speed;
- required resolution;
- cost-to-performance ratio;
- accuracy required;
- interface requirements;
- power requirements;
- physical dimensions.

The applications of A-D converters are numerous and have increased at almost the same rate as their performance. Common applications include, among others, data acquisition, measurement systems, analytical and medical systems, and filter control. A typical application: an A-D convertor-to-microprocessor interface, here between a PMI ADC-9012 and a 6502, is shown in Fig. 8. The circuit is fairly straightforward, except that the two LSBs are connected to data bits DB2 and DB3. The ADC-9012, a 10-bit 6 µs converter, makes special provision for this. A suitable interrupt service routine flow diagram is shown in Fig. 9.

Peak detection is one field of applications not usually associated with A-D converters, but it has become feasible with Ferranti's 8-bit converter Type ZN425E, which has an 8-bit counter on board.

The circuit diagram of a basic implementation of this is shown in Fig. 10 – note that only a small number of external components is required. The comparator enables pulses from the trigger circuit to be clocked by the internal counter and this produces a ramp output until it attains the level of the analogue input. Although rather inaccurate in this particular configuration, the circuit can be readily modified by the use of higher resolution A-D converters.

The AD7820 is a 1.36 µs, 8-bit microprocessor compatible A-D converter that has the advantage of not requiring user trims. The circuit shown in Fig. 11 enables a 9-bit resolution to be obtained by the use of two of these devices: full microprocessor interfacing is provided. Usually, this type of circuit is of limited application, because of its significantly increased chip count and cost if increases in resolution of more than a few bits are required. Nevertheless, this type of configuration is still worth considering in applications where either the cost or availability of a more conventional single-package solution would prove prohibitive.

References

Data Conversion Products Handbook – Analog Devices, 1988.

Data Converters and Reference ICs – Ferranti Semiconductors, 1986.

Data Conversion Handbook – PMI, 1988; Datel, 1988; Sipex 1988.

ELECTRONICS SCENE

Towards universal skyphones

INMARSAT, the International Maritime Satellite Organization, has joined forces with the International Civil Aviation Organization (ICAO) to plan and provide airborne satellite communications for both airliner crews and their passengers.

INMARSAT, a global satellite operator with investors from 56 countries, provides mobile communications world-wide. Almost 9,000 ships and land transportable units currently use the the INMARSAT Standard-A satellite communications system for direct-dial telephone, telex, facsimile and data communications. INMARSAT has offered a similar range of services for aircraft after the first commercial satellite phone call from an aircraft last February.

ICAO is the international regulatory body for civil aviation matters.

The new agreement confirms the capability of INMARSAT to offer mobile satellite communications services in support of air traffic services, airline operations and administration, and passenger communications. It also recognizes ICAO's exclusive competence to establish international standards and recommended practices in aeronautical communications.

New computer speeds up overseas mail

A new computer system, the Tatom (Tracking and Tracing of Overseas Mail), has been taken into use by the British Post Office.

Tatom gives information about flight schedules and cargo space, matches the demand with available space, determines the fastest routes, and tracks every mailbag with a bar code label.

Since this is the way all major European countries want to go, the Post Office expects that eventually there will be a total link-up of all the computers of all the post offices. Already, talks are underway between the world's major post offices to use the system to privide full control of mail movements world-wide.

Old recordings as good as new

The bumps, scratches and hiss on early recordings can now be eradicated entirely by a new process developed by musicians and computer experts at Cambridge Sound Restoration.

Cedar (Computerized Enhanced Digital Audio Restoration) can be applied to any material used for recordings, such as wax, vinyl or film, by digitizing the original sound, removing the extraneous noise aand giving the listener the exact unmuffled performance.

Cedar's first success was with a 1953 performance of Gustav Holst's *Planet Suite* by the London Philharmonic Orchestra conducted by Sir Adrian Boult. The recording was marred by hisses, cracks and thumps and something like a potato fryer sizzling away in the background. The restored disc is clear and noise-free, sounding as pristine as when it was first made.

All other known noise-eradicating processes use some kind of filtering that automatically affects the sound signal as well as the offending hiss and scratches, but Cedar gives the true performance.

Cedar was invented by Cambridge Sound Restoration (CSR) and is closely tied to the British Library's National Sound Archive.

At the request of the National Sound Archive, Dr Peter Raynor, whose research work at Cambridge University is the basis of Cedar, used a computer to distinguish between signal and noise on a recording. He then developed a set of algorithms to separate the noise without affecting the signal. Where the signal itself was flawed, he perfected an interpolation algorithm. This enables the computer to analyse the signal on either side of the flaw and calculate the most likely waveform to fill the gap. The result is that even records that have been broken can be glued together and treated by the process, providing the break is clean.

Because each piece of music or speech recording is different, a diverse set of problems is presented each time, which means that Cedar is being refined constantly. The most striking advance since the company's formation last February is the speed of the process. Initially, it took about 24 hours to process a few minutes of recording. Now it takes only slightly longer than the recording itself.

There are enough old recordings to keep CSR busy for a long time. The National Archive alone has more than one million items, while the BBC and record companies have virtually every recording since the gramophone was invented in 1877.

FROM THE SATELLITE-TV DESK

with a contribution by P.N.P. Wintergreen

In line with this month's theme, Satellite and Cable TV, sundry matters are discussed that relate to our recent publications in the increasingly popular field of satellite-TV reception.

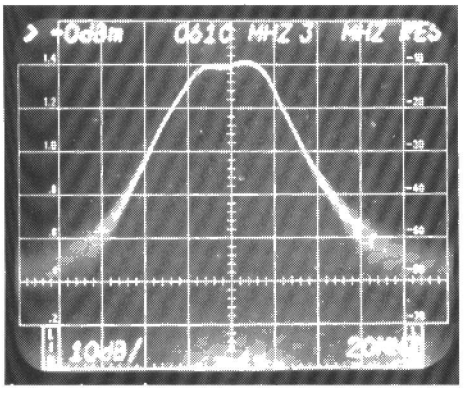
Astra on the Indoor Unit

The numerous constructors of the Indoor Unit for Satellite TV Reception (Ref. 1) will be pleased to learn that it is fairly simple to modify this receiver to accomodate the channel bandwidth used by the 16 transponders on the Astra-1A medium-power TV satellite at 19.2 degrees East.

The IF amplifier, composed of active elements T_2, IC_1 and T_3, provides about 42 dB gain at a centre frequency of 610 MHz and a 3 dB bandwidth of about 36 MHz, as required for communication satellites in the ECS and Intelsat series. The Astra-1A, however, uses a channel bandwidth of 27 MHz. Since the receiver is 36 MHz wide, reception of Astra-1A often gives rise to interference between adjacent channels. Fortunately, the problem is simple to resolve by reducing the bandwidth of band-pass filters L_3-L_4 and L_6-L_7. Cut two 3 mm high, 20 mm long pieces of tin plate or brass. One of these pieces is soldered vertically between L_3 and L_4, the other between L_6 and L_7. The screens prevent the inductors 'seeing' each other, and change the coupling from inductive to capacitive via the trimmers at the RF side of each line inductor.

The results of this modification are shown in the photographs of Fig. 1: the IF bandwidth has been reduced by about 8 MHz, which solves all problems in the reception of Astra-1A. Note that the IF centre frequency change from 610 MHz to 595 MHz is irrelevant to the operation of the receiver, since the PLL and IF filters can be adjusted accordingly.

During the re-adjustment the IF amplifier for the lower bandwidth, the spectrum analyser indicated out-of-band oscillation at about 700 MHz. Fortunately, this troublesome effect proved simple to eliminate by fitting a resistor in series with the input of the hybrid IF amplifier, IC_1. Cut the track from pin 1 to C_{12} close to pin 1, and remove some copper at either side to make room for a 10 Ω chip resistor that must be soldered direct on to the track ends.



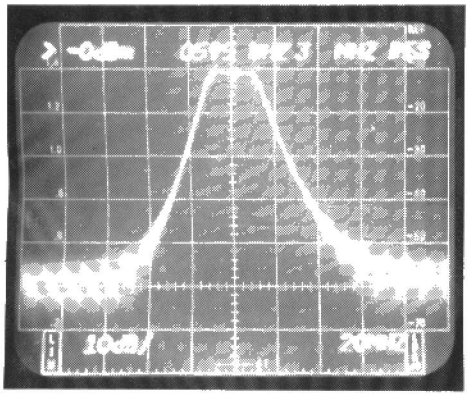
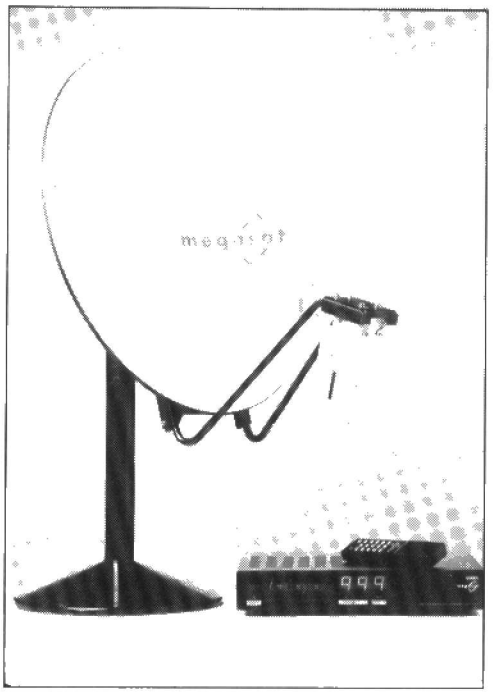


Fig. 1. Pass-band curve of the unmodified IF amplifier (*BW* = 36 MHz; top photograph) and that of the modified version (*BW* = 28 MHz; lower photograph).

Filmnet decoder and Amstrad SRX receiver

At the time the Filmnet decoder (Ref. 2) was published, it was not known whether the SATPAK scrambling system employed on the ECS-4 would be used for Filmnet's transmissions on Astra-1A as well. We have now learnt that this is the case, so that owners of an Astra-compatible receive system can confidently build the Filmnet decoder and watch the programmes on channel 11.

The Amstrad SRX200 indoor unit has a 15-way sub-D connector for future extensions such as a Eurocrypt or Videocypher decoder. This connector, whose pinning is largely standardized among manufac-



Megasat's System 7000 uses a 60 cm dish and a Uniden indoor unit.

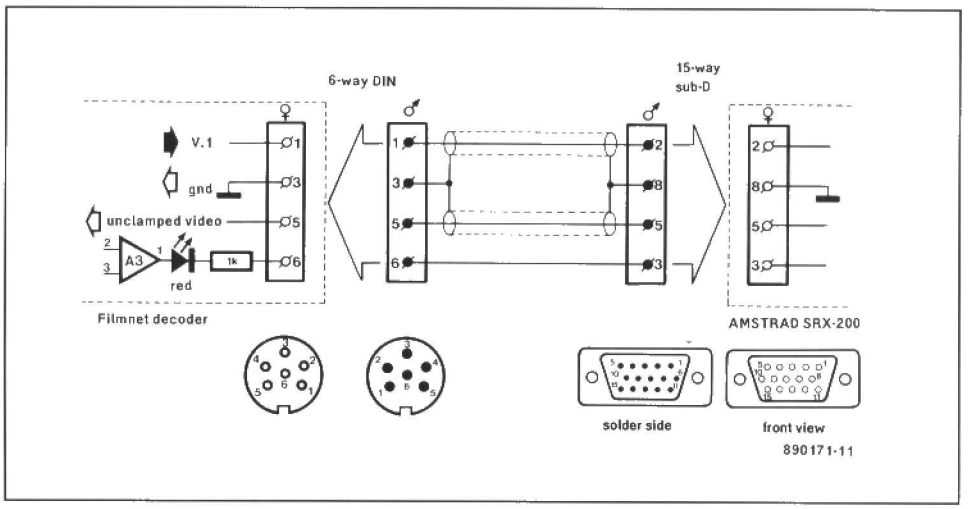
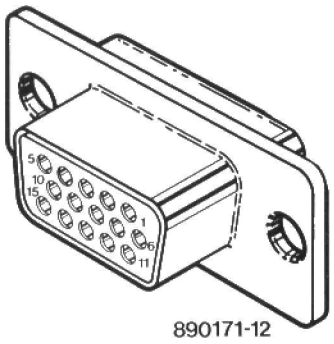


Fig. 2. Connections between the SRX200 Astra receiver and the *Elektor Electronics* Filmnet decoder.



1 audio return L .....500–700 mV into 10kΩ
2 video return.....1 Vpp into 75Ω
3 video control voltage ...0 V or +12 V
4 baseband output .....25 Hz – 10.5 MHz
.....(–3 dB)
5 video output.....1 Vpp into 75Ω
6 audio return R .....500–700 mV into 10kΩ
7 audio control voltage ...0 V or +12 V
8 ground
9 spare
10 spare
11 ground
12 audio output L .....500–700 mV into 10kΩ
13 audio output R.....500–700 mV into 10kΩ
14 spare
15 spare

Fig. 3. Pinning and signal assignment of the INTERFACE connector at the back of the Amstrad SRX200 Indoor Unit.

turers of Astra receiver sets, is marked INTERFACE in the case of the SRX200 (Fig. 3). The mating 15-way 'high-density' plug should be available from your satellite-TV dealer.

The combination of the Filmnet decoder and the SRX200 gives excellent results when the units are connected as shown in Fig. 2. The inputs of the video processing circuitry and the 7.56 MHz NBFM pulse receiver in the decoder are connected as shown in Fig. 11 in Ref. 2. The common input is driven with the unclamped video signal available at INTERFACE connector pin 5. A 500 Ω preset is fitted at the input of the video board of the Filmnet decoder to enable the video output level to be set to 1 V_{pp}.

The home-made screened cable is about 75 cm long, and enables automatic switch-over and video rerouteing by the use of a control input on the SRX200. When taken to +12 V, this input causes the video circuitry in the SRX200 to switch over to the decoded Filmnet signal applied to pin 2 of the INTERFACE connector. A 6-pin 270° DIN connector is used at the decoder side of the cable. The pinning is arbitrary.

Two components, a LED and a resistor, are added to the decoder (see Fig. 2). The combination is connected to the output of opamp A_3, which functions as the driver for the 'encoded' LED. The added LED does not function as an indicator but as a 1.4 V zener diode. It must, therefore, be a red 5 mm type to ensure the correct forward drop.

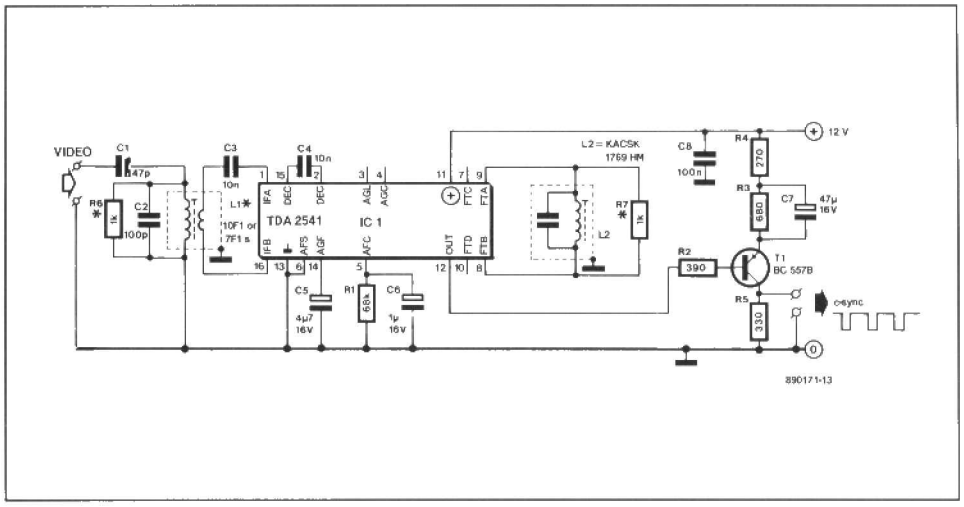


Fig. 4. Circuit diagram of a composite-sync pulse demodulator for cable networks. The chip used is actually an AM video demodulator .

Filmnet decoder and cable networks

Many readers from continental Europe have requested information on the conversion of the Filmnet decoder for use with their radio & TV cable network.

AM pulse receiver

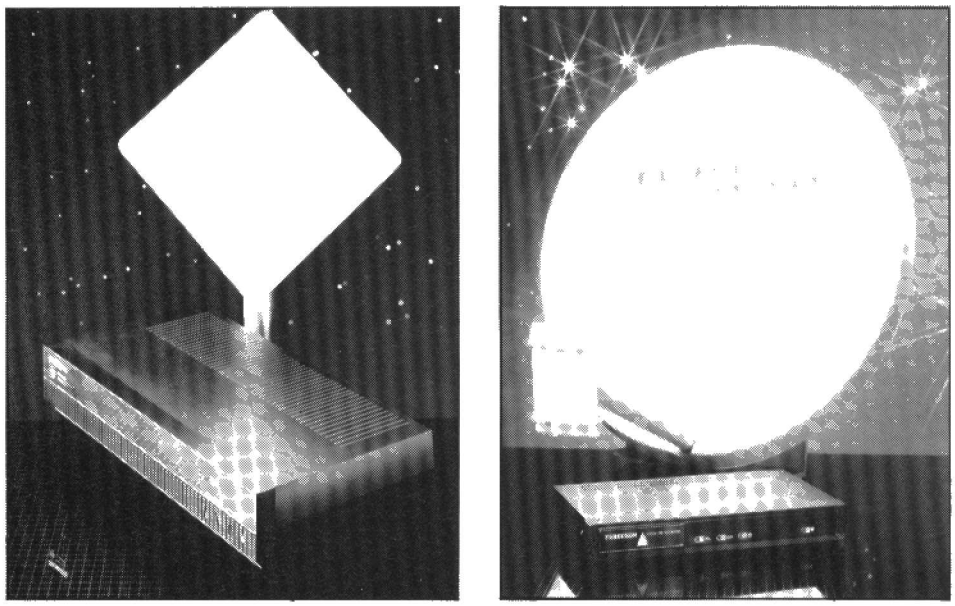
Although details of the operation of the SATPAK scrambling equipment on cable networks are given in Ref. 2, a brief summary is given here.

On most cable networks, the c-sync pulses are amplitude-modulated on to the frequency-modulated sound subcarrier at 5.5 MHz (6.0 MHz in the UK and some other countries). The 7.56 MHz NBFM pulse receiver used with an indoor unit is, therefore, not required if you have a cable connection.

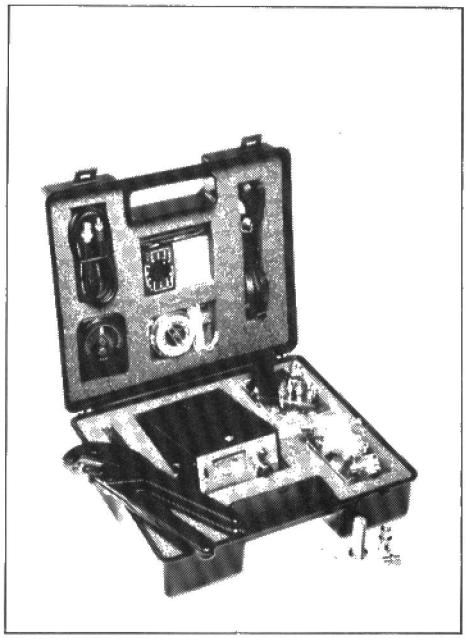
A suggested circuit of an AM pulse receiver is shown in Fig. 4. The input of the demodulator is driven by the video signal (scrambled or descrambled), which usually contains a strong enough 5.5 MHz component to enable driving the sensitive AM pulse receiver. Inductor L_1 is a home-made type dimensioned for resonance at 5.5 MHz. It is damped by R_6 to prevent FM demodulation. The primary of L_1 has about 10 turns, the secondary about 50. The wire used is dia. 0.1 mm enamelled copper.

The demodulator chip, a Type TDA2541, is quite sensitive, so that high signal levels are not required at the balanced input. Inductor L_2 is a ready-made type from Toko with a built-in parallel capacitor. This inductor is also damped for the same reason as L_1. The values of the damping resistors may have to be changed to eliminate spurious pulses at the c-sync output owing to the frequency-modulated sound on the 5.5 MHz subcarrier.

Collector follower T_1 feeds the inverted c-sync pulses to the relevant input of the



Two Ferguson satellite TV reception packages: to the left the SPB1 with a 'squarial' flat-plate antenna for BSB reception, and to the right the SAP1 for Astra reception.



Perhaps one of the more useful novelties shown on the recent Cable & Satellite exhibition: Connexions' Professional Satellite Installation Kit. The kit comprises an inclinomter, a multimeter, an insertion tool, F-type 2-way splitters, F-type couplers, and an N-to-F adaptor.

decoder. The amplitude of the c-sync signal should be about 0.5 V_{pp}. If required, the demodulator can be modified for operation at 33.4 MHz (38.9 – 5.5) simply by fitting the appropriate inductors.

Pulse shifter

Logic circuitry in the head-end station of most cable networks shifts the position of the sync pulses to where their regenerated counterparts should be in the decoded signal. The c-sync timing is, therefore, different from that used on the satellite, as shown in Fig. 5c in Ref. 2. A small circuit is required to compensate the shift — see Fig. 5. The 1n capacitor is connected to pin 15 of IC_{19}. The connection between pin 15 of IC_{14} (RST input) and pin 4 of IC_{20} (N_{10}) on the main decoder board is broken, and the collector of the BC547B is connected to pin 15 of IC_{14}. The preset is carefully adjusted until the timing of Fig. 5a is achieved.

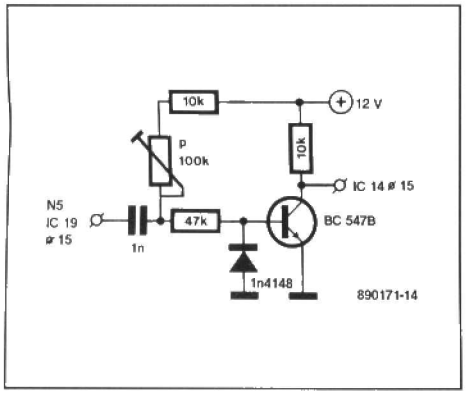


Fig. 5. This little circuit corrects the timing of the c-sync pulses as they are received from the cable network.

Line-up

In conclusion, these are the units and circuits required to get the Filmnet decoder to work from a cable network:

- A TV tuner plus IF unit. The tuner is tuned to the Filmnet channel (VHF or UHF) used on the cable network. It has been modified to supply an **unclamped** video signal of 1 V_{pp}, whose polarity is, in principle, irrelevant as it is automatically corrected by the decoder. If the video signal is clamped in any way, or non-linear, the decoder will supply a flickering picture. Suitable tuners and IF units are usually available from electronic surplus stores.
- The circuit of Fig. 4. The input is connected via screened cable to the video output of the tuner.
- The circuit of Fig. 5.

Further details on signal levels, modifications, adjustments and connections are hard to give because there are many different types of surplus tuners and IF modules around, all of which pose their own typical problems as to the disabling of the video clamping circuitry and the modification of the AGC (automatic gain control) constant. Also, the c-sync timing discussed above may be quite different on your cable network.

In conclusion, the conversion of the Filmnet decoder for use on a cable network requires quite some skill in working with RF and video circuits and is, therefore, not to be taken lightly.

References:

1. Indoor Unit for Satellite-TV reception. *Elektor Electronics* October 1986, November 1986, January 1987.
2. ATN-Filmnet decoder. *Elektor Electronics* March 1989.

Some useful addresses:

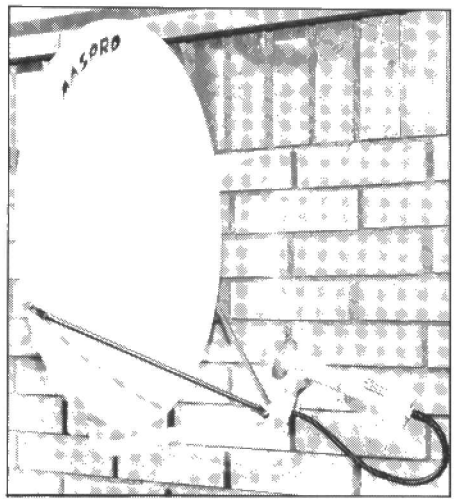
Connexions (UK) PLc • Unit 3 • South Mimms Distribution Centre • Huggins Lane • Welham Green • Hertfordshire AL9 7LE. Telephone: (07072) 72091. Fax: (07072) 69444. Telex: 295181.

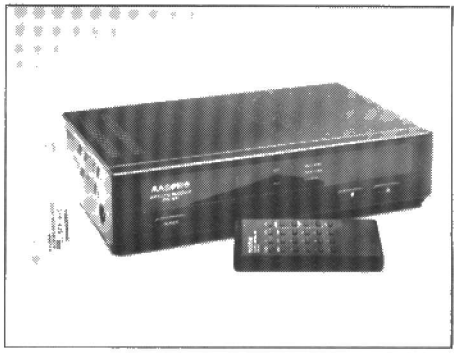
Cambridge Computer Ltd. • Bridge House • 10 Bridge Street • Cambridge CB2 1UE. Telephone: (0223) 312182/323268.

For Maspro products please contact Micro-X • Unit 2 • Drury Way Industrial Estate • Laxcon Close • London NW10 0TG. Telephone: (01 459) 1200. Fax: (01 459) 0110.

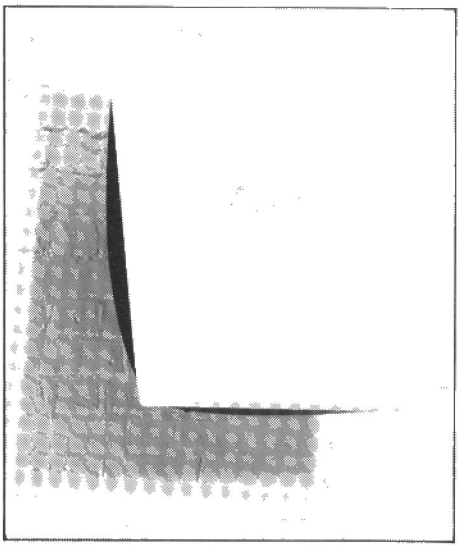
Megasat Ltd. • 5 St. Pancras Commercial Centre • Pratt Street • London NW1 0BY. Telephone: (01 267) 5222. Telex: 94015803 MEGA G. Fax: (01 485) 1342.

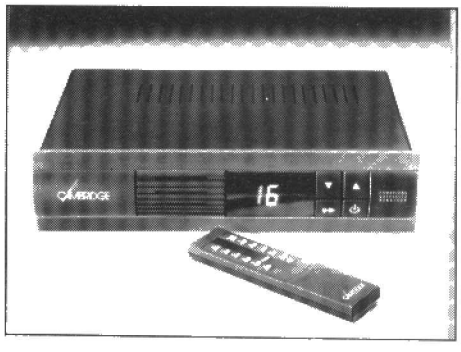
Ferguson • Cambridge House • 270 Great Cambridge Road • Enfield • Middlesex EN1 1ND. Telephone: (01 363) 5353. Telex: 916304 FERG G.





Maspro's 65 cm offdet dish and SRE90R indoor unit. The receiver features 50-channel capability, remote control handset, parental lock facility, 12-programme storage, and a skew facility.





The new 60 cm Cambridge dish and associated set-top receiver with stereo output.

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	890007-2	2.15	0.33
	890007-3	8.35	1.26
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